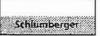
# 7081/7071 DIGITAL VOLT METER

# Maintenance Manual

Issue 5: August 1986

Part No. 70810014



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Schlumberger pursue a policy of continuous development and product improvement. The specification in this document may therefore be changed without notice.



# 7081/7071 DIGITAL VOLT METER



#### SAFETY

These instruments have been designed and tested in accordance with the recommendations of IEC 348 Class 1. They are primarily intended for indoor use, and for such use are supplied in a safe condition. However, no degradation of their safety will be caused if they are occasionally subjected to temperatures below normal room temperature.

This manual contains information and warnings which the user should follow to ensure his own safety and for the continued safe operation of the instruments. The 7081 and 7071 have been engineered with ease of use as one of the primary considerations. Attention has also been given to making the instruments immune to most inadvertent overloads. It should be appreciated, however, that even the most sophisticated measuring instrument can be dangerous when connected to high voltages, unless elementary safety precautions are observed.

The voltage limits of lkV on AC and DC mean that no damage will be caused to the instruments at this level of input. Other than the displayed reading, however, no indication is given to the user that a voltage of such magnitude is present at the input terminals. Care should therefore be exercised whenever dvm input leads are being connected to/removed from live circuits, especially where high voltages are known to exist, or high transients could occur.

Similarly, when using the instruments on mains operated equipment capable of delivering high voltage outputs, it is strongly recommended that the equipment under test is NOT switched off with a dvm still connected. For example, consider a 7081 connected across the secondary winding of a large mains transformer. The instruments very high input resistance is such that in the event of the mains supply being interrupted, the resultant back emf induced in the undamped secondary could be in the order of 100kV. This is obviously hazardous to the user and would certainly harm the voltmeter.

Whenever it is likely that the safety of the instruments have been impaired, e.g. if there are any visible signs of damage, failure to perform correctly, or if the specfications have been exceeded in any way, the instrument should be made inoperative and referred to a suitable repair organisation.

Any adjustment, maintenance or repair of these instruments should be carried out only by a skilled person who is aware of the hazards associated with mains operated equipment. Such adjustment, maintenance or repair should be carried out in accordance with the procedures, and observing the precautions, detailed in this Maintenance Manual.

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# CHAPTER 1

# General Information

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#### 1.1 INTRODUCTION

This manual contains technical information that is intended primarily to meet the needs of the service engineer. A detailed treatment of the principles of operation is not included but the descriptive text covering each circuit diagram is sufficient to enable the reader to understand the purpose of the circuit and its effect on its input(s). To facilitate fault diagnosis, attention is drawn to peculiarities of circuits, together with any precautions necessary when carrying out checks.

Both the 7081 and 7071 have identical electronic circuits. This means that all the circuits diagrams included in this manual are valid for both instruments. The difference between these two instruments exists primarily at the software level, and on the higher specification components required by the 7081. The 7081 undergoes a significantly more rigourous quality control proceedure.

#### 1.2 PRESENTATION OF INFORMATION

The circuit diagrams are arranged to fold out clear to the right. Signal paths are indicated by bold lines, arrows being used where necessary to indicate the direction of functional flow. In general this is from left to right, feedback paths flowing from right to left. To prevent ambiguity, however, and where space is limited, this convention has not been followed rigidly.

In addition to the circuit diagrams, lined drawings are reproduced in the manual to facilitate rapid identification of components during diagnostic checks.

#### 1.2.1 Power Rails

These are represented by short, detached bars annotated to show the nominal voltage. Several separate bars, annotated with the same voltage, may appear on a diagram. These are electrically connected to a common rail derived from the Power Supply circuits.

Note that voltages specified on the circuit diagrams are in all cases nominal values, the actual values being dependent upon the load offered to the supply by the specific circuit. Inconsistencies between actual measured values and those quoted should not, therefore, be regarded with suspicion without considering other symptoms of possible unserviceability.

#### 1.2.2 Split Pads

Split pads are used to provide a means of isolating various parts of the circuit for fault diagnosis. They are simply bridged with solder, open circuit being effected by removing the solder. It should be noted that excessive heat applied during this operation could damage the solder trace - a small, low wattage iron should be used.

#### 1.2.3 Test Points

A further aid to rapid circuit check-out is the provision of test pins. These are indicated on the circuit diagrams and clearly marked on the pcb's.

#### 1.3 PRINCIPLES OF OPERATION

The 7081 and 7071 employ an A-to-D Converter, which transforms the input voltage to a time analogue. This in turn is split into discrete, equal length time units, which are counted and the result displayed as a numerical indication of the measured quantity.

The V-to-T converter produces a pulse train, the pulse width being variable and proportional to the magnitude of the input signal. The pulses gate the output of a fixed frequency clock into a counter, over a time period which can be selected by the user. At the end of the time period, the total accumulated in the counter is a measure of the input during that time. An integrating technique is used whereby the total count is divided by the number of gating pulses used. The result obtained is displayed as a direct reading of the measured quantity.

Since the total count is much longer when operating at the longer integration times, the counter requires more capacity. This results in an increase in scale length and it follows that the display sensitivity is improved hand-in-hand with the increased measurement resolution.

#### 1.4 FUNCTIONAL DESCRIPTION

The circuits of the 7081 and 7071 can conveniently be divided up into four major functional sub-divisions:

- \* Signal Conditioning
- \* A-to-D Converter
- \* Digital Section
- \* Power Supply

An input is processed by the Signal Conditioning circuits, which convert all measured quantities into a dc voltage, scaled to a level suitable for further processing. Input protection, reference and guard circuits are included in this sub-section.

The correctly scaled dc signal is converted to a train of digital pulses by the A-to-D Converter, these pulses being used to gate the output of a Clock circuit.

Control of the measurement conversion and timing of the control sequences by the microprocessor set are two important functions of the Digital Section. It also contains the reversable counters which accumulate the gated clock pulses, and the latches which shift the counter contents to the databus.

The power supply provides all dc power for the instrument analog and digital circuits.

#### 1.4.1 Signal Conditioning

The A-to-D Converter is capable of handling dc volts only, regardless of the measurement being taken. Therefore, the Signal Conditioning circuits convert the input to a dc voltage level. Once converted, the input signal is applied to an amplifier, the gain of which is determined by the range on which the instrument is operating. The amplifier output is compared with the instrument's reference and both signals are applied to the A-to-D Converter.

#### 1.4.2 A-to-D Converter

The analogue input is converted to digital form by a circuit which produces a pulse train - the width of the pulses is proportional to the magnitude of the input. This technique is known as voltage-to-time conversion, the method employed being a variant in which "time" is in fact the difference between two distinct time periods. It is this differential which is used to control the number of clock pulses finally accumulated in an up/down counter in the Digital Section.

#### 1.4.3 Digital Section

The Digital Section comprises the phase comparator which produces the pulses that are counted to digitally measure the applied input; the microprocessor clock which supplies timing and synchronising signals for the digital circuits and a microprocessor set for controlling and shifting data.

The microprocessor set consists of two Central Processing Units and their associated memory devices as shown in Figure 1.1.

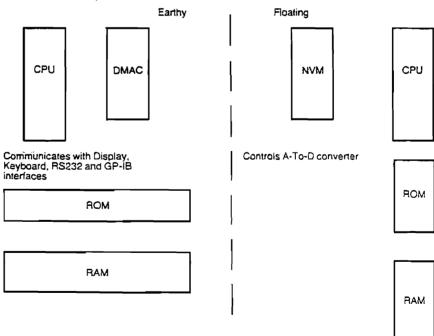


Figure 1.1 Microprocessor Set

The 'Floating' processor controls the A-to-D Converter and the range/mode drive circuits, and communicates with the Non-Volatile Memory (NVM) and the 'Earthy' processor. It has its own internal Read Only Memory (ROM) but also utilises external Random Access Memory (RAM) and ROM.

The 'Earthy' processor performs the following functions:

- \* communicates with the 'Floating' processor to command measurements.
- \* communicates with the Display, Keyboard, RS232 and GP-IB interfaces.
- \* calibrates results.
- \* controls the processing of results.
- \* controls the storage of results.

It has its own ROM and RAM set. In addition, some of the data movement is handled by a Direct Memory Access Controller (DMAC).

#### 1.4.4 Power Supply

The Power Supply features two pulse width-modulated switching regulators to provide both the "earthy" and "floating" supply rails. A mains transformer is used to connect the rear panel ac input to the regulators through full-wave rectifiers. A Power Fail Detect circuit is also included.

Note: The analogue boards (printed circuit boards 5 and 6) form a calibrated set and may be used with any other digital boards (and vice versa) provided that the software fitted is of the same issue and status. This is possible because the Non-Volatile Memory (NVM), which holds the calibration constants, is located on the analogue boards.

#### 1.5 FAULT DIAGNOSIS GUIDE

Owing to the complex nature of 7081/7071 circuits it is virtually impossible to document fully all fault conditions that might arise. However, it is possible to quickly narrow down a fault condition to a particular PCB, and sometimes to an area of just a few components. The following pages should prove especially useful since the comments are based firmly on the experiences of the 7081/7071 Test and Service Personnel.

Note: Sometimes an instrument may be suspected of being faulty because it gives 'wrong' or unstable reading. In cases like these, the fault quite often turns out to be a poor understanding of measurement techniques by the user. Before dismantling the 7081 or 7071, make absolutely certain during measurement or calibration that the proper precautions are taken to guard against interference, thermal emfs, high resistance leads, etc.

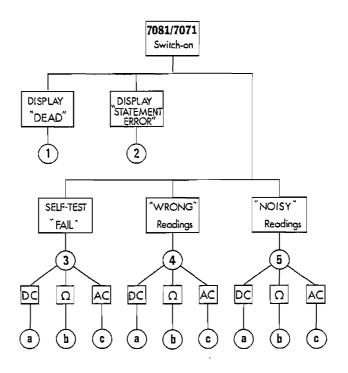


Figure 1.2 Fault Diagnosis Flow Chart

# 1.5.1 Display 'Dead' Check the +5V rail at D58 cathode, PCB3.

If the indicator lamps are also blank the fault could lie on PCB3 or PCB4. If substitute boards are available, use these to narrow down the search. The failure could be a MPU, DMA, RAM or ROM fault. Suspect ICs 401, 402, 406 to 411, 430, 412 to 415, or a display system fault on PCB3.

If the display shows incorrect symbols and figures, a PCB1 failure should be suspected.

#### 1.5.2 Display Statement Error

A correctly calibrated instrument must always show a RESUMED statement on power-up. Under error conditions, the following statements might be seen:

INITIALISED - This indicates that the NMI routine for retaining the history file at power-down was incorrect. Check the power supply of IC56; the battery circuit of PCB4 RAM.

CAL INCOMPLETE - This indicates that the NVM on PCB5 has not received all calibration constants following a calibration routine.

NVM FAIL - This could indicate a failure of the NVM circuitry, or of IC804. A spare NVM would prove useful here.

WAIT @ F - This could indicate a communication failure between the 'floating' and 'earthy' PCBs. Check IC9, IC10, IC11 or the clock of PCB3. On PCB5 check IC801, IC803, IC826 or the clock.

MAINS FAULT - This indicates that a mains character has not been received from the earthy side and would normally indicate a PCB5 failure. Check IC303, IC834, IC801. If the fault still persists, PCB3 must be suspected.

@F - This indicates that the WAIT @ F stage has been passed, but a fault probably exists in the 'floating' link. That is, in terms of the information flow between the 'earthy' and 'floating' circuits. The fault could lie on PCB3 or PCB5. Rarely, PCB4 or PCB1 could be faulty.

The fault is often due to a temperature sensitive IC and manifests itself after the instrument has been switched on for some time. It is difficult to localise this fault but it is more prevalent on PCB5. Check the floating logic sheet or V-T converter (sheet 1).

Suitable replacement boards and/or judicious use of a tin of freezer spray would not go amiss here.

#### 1.5.3 Self-Test Fail

A fail here usually indicates a major fault in the PCB 5 analogue section.

#### (a) DC

A fail of the OV test probably indicates a faul in the V-T converter stage (sheet 1), IC201, or the circuits associated with the RATIO circuit (sheet 3) of the integrator input.

If the OV test passes but shows a fail at 10V, a fault could lie in the input amplifier which prevents the 10V reference level from being fed to the V-T converter.

#### (b) OHMS

If a  $k\Omega$  fault is indicated check that there is:

- approximately 20V across R604
- (ii) approximately 6V across F609.

If either of these is wrong suspect IC601 or IC602. Failing these, check TR610 and the circuits around IC604.

#### (c) AC

Where an AC fail is indicated it is beneficial to check the AC level at TP705 to see whether the fault lies in the AC buffer or the AC converter. As an approximation, with IV, lkHz applied to 7081/7071 input, range IV, TP705 should be IV rms. The corresponding level out of the converter should be 5VDC (@ TP757).

#### 1.5.4 'Wrong' Readings

#### (a) DC

With a shorting-plug applied to the instrument input check the ranges 10V to 0.1V. If the indicated zero error gets larger as the range is reduced this indicates a fault in the chopper channel of the input amplifier. Check operation of IC101, IC104, IC401, IC404, IC405, and TR404.

If a constant error appears on all ranges suspect the V-T converter (sheet 1), IC201 or the input switching circuits to SP201.

If the zero readings are correct but the scaling of the readings is wrong (with an input applied) firstly check that the correct level is being applied to the V-T converter at SP201. If the level is correct check the reference voltage supplies (±10V).

#### (b) OHMS

A failure to provide correct resistance readings is usually due to incorrect levels at TP601 or TP603. The fault could lie in IC601, IC602, IC605, TR601, or TR602. If these are fine then check IC604, IC606, TR610, TR605, and D605.

#### (c) AC

Reference to section 6.7.1 can usually indicate the area of failure. If the system is basically working but the readings are incorrect then the various gain defining resistors could be suspect: R725, R750, R751a and R751b.

#### 1.5.5 Noisy Readings

#### (a) DC

Noisy readings on the 0.1V range are especially indicate of a noisy component in the input amplifier. Suspect component in the input amplifier. Suspect components D403, TR401, TR412, IC401. If the 10V range is also noisy (with short circuited input) then IC201 is a likely cause.

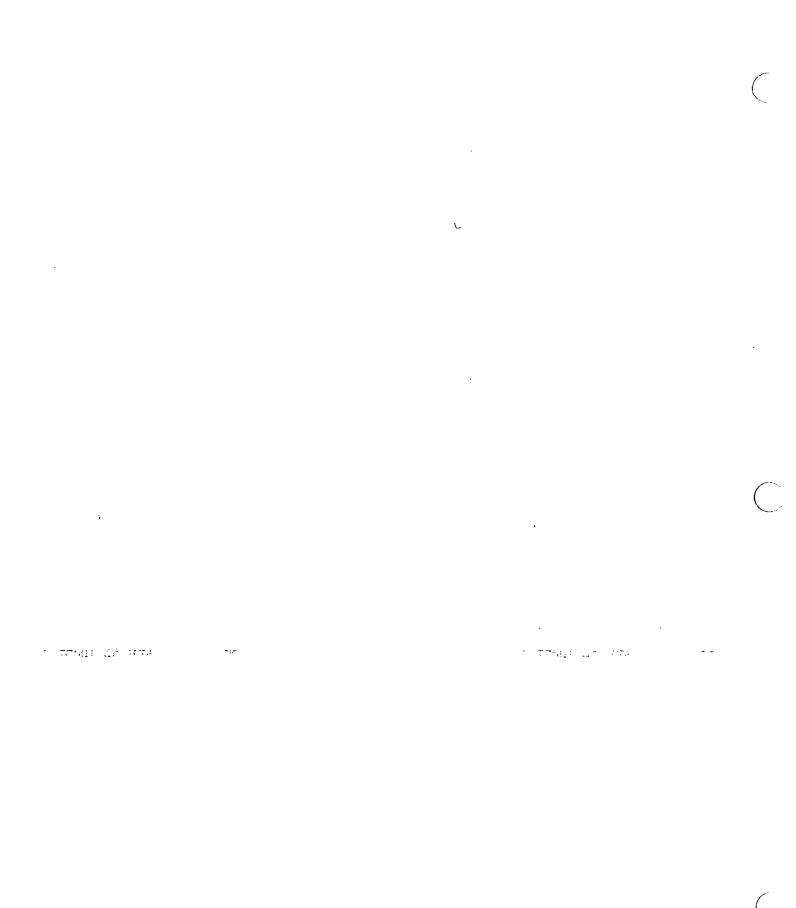
#### (b) OHMS

Noisy readings on the  $k\Omega$  ranges when the DC ranges are normal could be caused by IC601, IC602, IC603. Also D601, D602, D616, D617 could produce noise if they become 'leaky'.

#### (c) AC

If the AC readings are noisy the switching circuits around TR758 and TR759 could be at fault. Unstable readings could be produced by a breakdown by any of the FETs TR770 to TR779. By applying an input of approximately IV @ lkhz to input, and heating up the FET's individually with a hot-air gun (never apply direct heat to a component!), the fault may be quite quickly found by examining the display for any unreasonable large change in value.

The setting of the balance control RV751 is quite critical to ensure a minimum of noise on the AC readings. See Test Procedure for the correct adjustment of this pot.

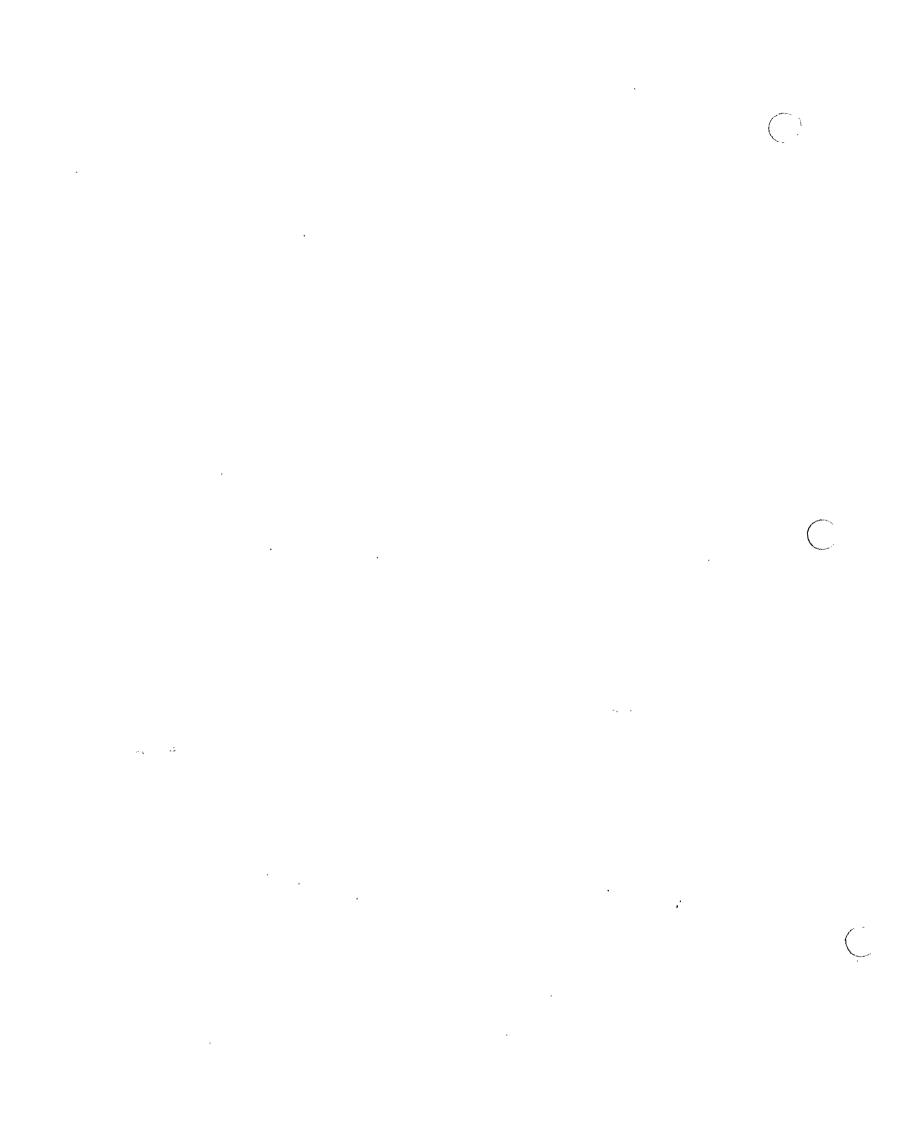


# CHAPTER 2

# Printed Circuit Board 1

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#### 2.1 INTRODUCTION

This printed circuit board permits processed data to be digitally displayed and the front panel annunciators to be lit as required.

#### 2.2 DATA INPUT

Processed data enters the printed circuit board via PL101, pins 14 to 21, and is applied to octal D flip-flops IC101 and IC102. IC101 is clocked by EDATSTB- and IC102 by ODATSTB-. On the rising edge of the clock signals the data is transferred to the Q5 outputs of IC101 and IC102 from where it is fed to both the Annunciator and the Display circuitry.

#### 2.3 ANNUNCIATORS

The Q outputs of IC101 and IC102 are applied to the D inputs of IC110/111 and IC112 respectively. IC110 to 112 are controlled by the BLANK+ signal such that, when BLANK+ goes to logic 0, a rising clock edge causes the D inputs to be transferred to the Q outputs to light the LED annunciators. IC111 and IC112 are clocked by one  $\overline{Q}$  output of IC106 and IC110 is clocked by the other  $\overline{Q}$  output.

#### 2.4 ANNUNCIATOR CLOCK SIGNALS

IC106 is driven by the Serial Data Ouput from Display drivers IC107 and IC108.

The serial data is applied to the D input of IClO6 and transferred, upon a rising 4800Hz clock edge, to the Q output. The inverse of the data signal also appears at the Q output and is used directly to clock ICll1 and ICll2. The Q output is applied to the D input of the second stage of IClO6. On the next rising clock edge, the inverse of the original IClO6 input appears at the  $\bar{Q}$  output and is used to clock ICll0. ICll0 is delayed by one 4800Hz clock cycle with respect to ICll1 and ICll2.

IC110 to IC112 are used to drive the annunciators indicated in Table 2.1.

Table 2.1 Annunciators

IC	Annunciator
110	NULL ON, SAMPLE, TRACK, TALK, LISTEN, PROGRAM
111	5x9, COMPUTE, LOCAL, SRQ, 6x9, 7x9, 8x9, DIG FILT; [7081] 4x, COMPUTE, LOCAL, SRQ, 5x, 6x, 7x, DIG FILT; [7071]
112	$$ , $\sqrt{-}$ , $-$

#### 2.5 DISPLAY

The Q outputs from IC101 and IC102 are applied, via Buffers IC104 and IC105, to the Display, DS101. This display is controlled, via its grid inputs, by Display Drivers IC107 and IC108.

DSPDAT+ is applied to the Serial Data Input of IC108. On a rising edge of the 4800Hz signal, DSPDAT+ is transferred to IC108's internal shift registers. When the BLANK+ signal falls to logic 0, the data signal is passed out of the device, via its parallel output pins, to the grid inputs (Gl to 10) of DS101.

The Serial Data Output from IC108 is applied to the Serial Data Input pin of IC107. IC107 operates in exactly the same fashion as IC108 except that there is a delay, with respect to IC108, of one clock pulse. The parallel outputs from IC107 are applied to the grid inputs (G11 to 20) of DS101.

Serial Data Output from IC107 is applied to the D input of IC106 as described under 'Annunciator Clock Signals'.

The anode inputs to DS101, i.e. inputs a to n, ',' and '.', denote which segment of the display digits is to be lit (see Figure 2.1). The grid inputs denote which of the twenty digits are to be lit.

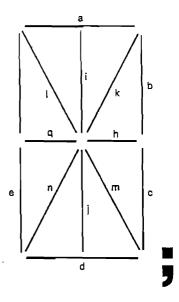


Figure 2.1 Display Segments

DS101 lights when the grid and anode inputs are positive with respect to the filament inputs. Fl and F2 supply the filament inputs to DS101.

CAUTION: The outputs of IC107 and IC108 are rated at 40V maximum. Care must be taken when probing these ICs not to connect an output to an input pin as the inputs are rated at only 5.5V maximum.

### CHAPTER 3

## Printed Circuit Board 3

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#### 3.1 INTRODUCTION

Printed circuit board 3 contains the main power supplies; the floating link, which provides the interface between the 'earthy' and 'floating' circuits; the microprocessor clock and reset circuits; and the RS232. Minate, Keyboard and Display interfaces. Figure 3.1 shows the interconnection between these circuits.

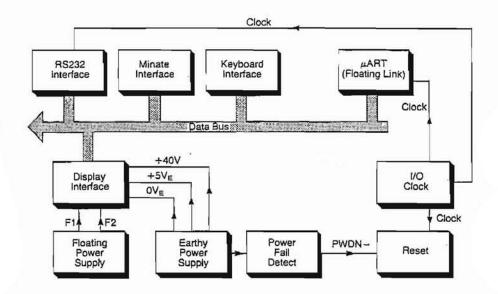


Figure 3.1 Printed Circuit Board 3 Interconnections

#### 3.2 FLOATING LINK (Sheet 1)

A 7081 or 7071 is controlled by two microprocessors, one on the floating side and one on the earthy side. The two processors communicate through a two-wire serial link, which is optically isolated by IC10 and IC11. On the earthy side, the link is serviced by a UART, IC9. This operates under DMA control when receiving and under program control when transmitting.

#### 3.2.1 Link Handshake

To ensure that the earthy and floating processors stay in step, all messages sent through the link are acknowledged. The processor which receives a message replies with a single character.

An exception to the single character reply occurs when new commands are sent by the earthy processor to the floating processor. In this case the single character is replaced by the new command. New commands are sent to the floating processor only when it is expecting an aknowledgement.

#### 3.2.2 Wakeup

To keep the earthy side aware of the overload status of the analogue circuitry when the instrument is not measuring, the floating side prompts single glug integrations at 50ms intervals. Range information is sent also so that the earthy side can keep track of the analogue range during auto-range operation.

#### 3.2.3 Negative Acknowledge

Most errors that may occur on the floating link can be detected by the receiving processor, which responds with a negative acknowledgement.

The DMA is allocated a buffer for the received characters and if an attempt is made to use more buffer space than that allowed (buffer overflow) a 'float full' interrupt (DMA FL INT-) is generated. A 'float full' interrupt is also generated if a negative acknowledgement (which is a request to resend) is received from the floating side. The two error conditions are distinguished by the state of the 'float receive single' flag, which is set if a single character is expected (negative or positive acknowledgement). A buffer overflow results in a negative acknowledgement. A negative acknowledgement sets a flag which prompts a resend of the last message after a finite period of time.

The receipt of an End of String (EOS) generates an EOS Interrupt, which causes the received message to be inspected. Each character is placed in the buffer with a status byte that indicates whether or not the character was received correctly.

#### 3.2.4 Power Up Sequence

The floating side is pushed out of reset by a character sent from the earthy side. This then displays WAIT @ F.

As part of its reset procedure, the floating side determines the mains frequency and sends one of three characters denoting the frequency to the earthy side. If the character sent is unrecognised, the system goes to the floating reset state and MAINS FAULT is displayed.

If the mains character is valid, the floating side begins by presetting the hold-off counter. To do this it forces a hold-off message to the earthy side. Instead of giving a positive acknowledgement the earthy side sends a new command, i.e. DUMP, NVM. This starts a succession of messages from the floating side, all of which are acknowledged. An NVM or calibration state message is then displayed. Or, if the NVM DUMP has been successful, RESUMED or INITIALISED is displayed.

#### 3.3 RS232 INTERFACE (Sheet 1)

The RS232 Interface circuit consists of the asynchronous communications interface adaptor (ACIA), ICl9, buffers and drivers, IC4, IC25, and interface connector SK3.

The ACIA (ICl9) provides a means of efficiently interfacing the microprocessor on printed circuit board 4 to devices requiring an asynchronous serial data format.

In the transmission of asynchronous data, no pre-synchronised clock is provided with the data. Also, the gaps between the data characters require that synchronisation be re-established for each character. Therefore, the receiving device must be capable of establishing bit and character synchronisation from the characteristics of the asynchronous format. Each character consists of a specified number of data bits preceded by a start bit and followed by one or more stop bits. The purpose of the start bit is to enable a receiving system to synchronise its clock to this bit for sampling purposes and thereby establish character synchronisation. The stop bit is used as a final check on character synchronisation.

The microprocessor processes eight bit parallel bytes that do not include start and stop elements. Therefore, serial data received in an asynchronous format must be converted to parallel form with the start and stop elements stripped from each character. Likewise, in order to transmit serial data, the parallel data byte from the microprocessor must be converted to serial form with the start and stop elements added to each character. This serial-to-parallel/parallel-to serial conversion is the primary function of IC19.

Data flow between the microprocessor and ICl9 is via 8 bidirectional lines, D0 through D7, that interface with the microprocessor data bus. The direction of data flow is controlled by the microprocessor via the Read/Write (R/W) input to ICl9.

ICl9 is enabled by a logic 0 signal (\$4800) applied to its CS2 input. Specific registers within the ACIA are selected by the A0 signal applied to its Register Select (RS) input. The microprocessor can read or write into the internal registers by addressing the ACIA, via the address bus, using these two input lines.

The microprocessor also applies a timing signal to the ACIA via the Enable input. The Enable (E) pulse conditions the ACIA's internal interrupt control circuitry and times the status/control changes.

The RS232 side of IC19 is configured as a DCE (data communications equipment) and is normally connected, via SK3, to a DTE (data terminal equipment) without an intervening modem link. Pin 2 of SK3 is marked TxD to indicate the path of data transmitted by a terminal to the instrument; Pin 3 is marked 'RCVD' to indicate the path of data received by a terminal from the instrument. Pins 5, 6, 8 and 20 are linked together inside so that a terminal sending DTR (data terminal ready) receives back the enabling states of CTS (clear to send), DSR (data set ready) and DCD (data carrier detect) whether the 7081 or 7071 is ready or not.

The Tx and Rx Clock inputs are both tied to the output of the MPU clock circuit on IC8 pin 6.

IC19 requests an interrupt to the microprocessor via its IRQ-output, which is applied to the Interrupt circuitry of IC13 as RS232INT-.

The pin/signal assignments for the RS232 connector are given in Table 3.1.

Table 3.1 RS232 Connector Pin/Signal Assignments

Pin No.	Signal
1	Ground
2	Transmit Data (TxD) - Input to 7081 or 7071
3	Receive Data (RCVD) - Output from 7081 or 7071
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
7	0V
8	Data Carrier Detect (DCD)
20	Data Terminal Ready (DTR)

#### 3.4 MINATE INTERFACE (Sheet 1)

The Minate Interface consists of peripheral interface adaptor (PIA) IC20, MOSFETS TR6 and TR7, and interface connector PL4.

When IC20 is enabled by a logic 0 \$5400 signal to its  $\overline{\text{CS2}}$  input the data flows between the microprocessor and IC20 on the data bus, via eight bi-directional data lines (D0 through D7). The direction of data flow is controlled by the microprocessor via IC20 Read/Write (R/W) input. Two addressing inputs RS0 and RS1 are used in conjunction with a control bit within the PIA for selecting specific registers in IC20. The microprocessor uses these address lines and the R/W signal to write into the PIA's internal registers.

The microprocessor applies a timing signal to IC20, via the enable input. This signal conditions the PIA's internal interrupt control circuitry and also controls the timing of the peripheral control signals.

The interface side of the PIA includes two 8-bit bi-directional data buses (PAO-PA7 and PBO-PB7) and four Interrupt control lines (CA1, CA2, CB1 and CB2). All of these lines are TTL compatible. In addition, all lines serving as outputs on the B side of the PIA can supply up to lmA of drive current at 1.5V.

The outputs of IC20 are used as follows:

- \* lines PBO to PB7 are fed to the N.V. Clock circuit.
- \* lines PAO to PA7 and CA2, CB2 are fed to the Minate Connector,
- \* line CA2 is supplied to the gate of MOSFET TR6 to turn it on,
- \* line CB2 provides the same function for MOSFET TR7.

The pin/signal assignments for the Minate connector are given in Table 3.2.

Table 3.2 Minate Connector Pin/Signal Assignments

Pin No.	Signal
1	1
2	2
3	4
4	8 Device Control
5	10 Device Control
6	20
7	40
8	80
9	Contact closure remote trigger
10	Out of Limit high
11	Out of Limit low
12	OVE
13	+5V
24	TTL compatible digitise complete signal
25	lkV probe enable

#### 3.5 KEYBOARD INTERFACE (Sheet 1)

The Keyboard Interface consists of peripheral interface adaptor (PIA) IC21 and BCD to decimal decoder IC23.

When IC21 is enabled by a logic low \$4C00 signal applied to its CS2 input the data flows between the microprocessor and IC21 on the data bus, via eight bi-directional data lines (D0 through D7). The direction of data flow is controlled by the microprocessor via IC21 Read/Write (R/W) input. Two addressing inputs, RSO and RS1, are used in conjunction with a control bit within the PIA for selecting specific registers in IC21. The microprocessor can read or write into the PIA's internal registers by addressing the PIA via the system address bits using these input lines and the R/W signal.

The microprocessor applies a timing signal to IC21 via the enable input. This signal conditions the PIA's internal interrupt control circuitry and also controls the timing of the peripheral control signals.

The interface side of the PIA includes two 8-bit bidirectional data buses (PAO to PA7 and PBO to PB7) and one Interrupt control line, CB2.

Outputs PBO to PB3 of IC21 are connected to inputs A, B, C and D of IC23, the O to 9 outputs of which are connected directly to the instrument keyboard. Table 3.3 shows the logic states of these pins relative to the A to D inputs. Outputs PBO to PB3 are also connected to IC26 the N.V. clock chip.

The inputs of IC21 are used as follows:

- \* Line PB4 (lkV range select) is connected to the Minate interface connector.
- \* Lines PB5 to PB7 are connected to the RS232 switch to enable reading of the baud rate set.
- \* Lines PAO to PA4 are connected to the keyboard.
- \* Line PA5 is connected to the calibration switch on the instrument front panel.
- \* Lines PA6 and PA7 are connected to switch Sl for stimulus program activation.
- \* Line CB2 is connected to the Minate interface connector.

Refer to Table 3.4 for a listing of the Keyboard Matrix Connections.

Table 3.3 IC23 Logic States

D	C	В	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	Н	Н	Н	H	Н	H	Н	Н	H
L	L	L	Н	H	L	H	H	H	H	H	H	H	Н
L	L	Н	L	Н	H	L	H	H	Н	Н	H	Н	Н
L	L	Н	Н	Н	Н	H	L	Н	H	Н	Н	H	H
L	Н	L	L	H	H	Н	Н	L	Н	H	H	H	Н
L	H	L	Н	H	H	Н	H	H	L	H	H	H	H
L	Н	Н	L	Н	Н	Н	H	H	Н	L	Н	Н	Н
L	Н	Н	H	H	Ħ	H	H	Н	H	Н	L	H '	Н
H	L	L	L	H	н	H	Н	Н	Н	H	Н	L	Н
Н	L	L	H	Н	Н	Н	Н	H	Н	H	H .	H.	L

L = logic low

Table 3.4 Keyboard Matrix Connections

1	lumn	PL2 Pin Numbers							
RO	w w	1	2	3	11	12	13		
P	б	٧	RATIO	TRU Ω	AUTO	DIG	NULL	HIST	SAMPLE
L						FILT	ON	→	
2 P	7	Ω	~+	~ FILT	PROG	SELF TEST	INITIAL- ISE	MEM	
N	8	V~	V		COMPUTE	LOCAL	SRQ		
N 0 S	9	6 x 9	5 x 9	Δ	7 x 9	8 x 9	NULL	HIST ←	TRACK

H ≈ logic high

DISPLAY INTERFACE (Sheet 1)
Display data from the data bus (lines D7 to D0) is applied through inverting line drivers (IC22) to the Display, via PL6 pins 14 to 21. Outputs D6, D5, D4, D1 from IC22 and D7, D3, D2, D0 from the data bus are applied to NAND gate IC24. If the EOS character appears during a receive DMA Bus cycle, the output from IC24 (end of string) is applied to IC3 in the interrupt circuitry to generate an EOS INT via IC16 Q output.

Chapter 4 includes a full description of the Display Interface operation in relation to the DMA.

Refer to Figure 3.3 for the display timing.

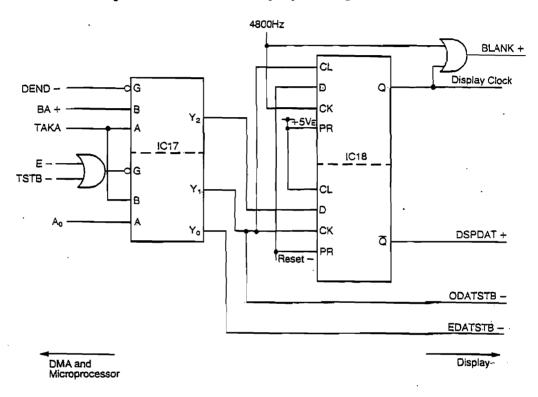
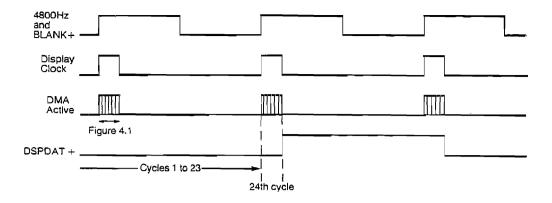


Figure 3.2 Display Interface



If the DMA fails, Display Clock will remain at logic 1 and the Display will be blanked

Figure 3.3 Display Interface Timing

#### 3.7 I/O CLOCK (Sheet 1)

A 1.2288MHz clock signal is generated by crystal Xl, Inverters ICl and associated components, and applied to the Clock input of part l of binary counter IC2. IC2 divides the signal by 8 to give 153.6kHz at its  $Q_{\rm C}$  output and by 16 to give 76.8kHz at its  $Q_{\rm D}$  output. The QC output signal is applied to IC8 D7 input, and the QD output signal to the D6 input of IC8, and to the Clock input of divider IC7.

IC7 divides the 76.8kHz signal to produce the following frequencies:-

- 38.4kHz to IC8 D5 input,
- 19.2kHz to IC8 D4, via inverter ICl and to IC2 part 2 Clock input,
- 9.6kHz to IC8 D3 input,
- 4.8kHz to IC8 D2. via inverter IC1.
- 2.4kHz to IC8 Dl input.
- 37.5Hz to provide a Clock signal for the Reset circuitry.

The 19.2kHz signal is applied to IC2 part 2. The QA and QB outputs are ANDed together in IC3 and the output applied to another part of IC3 along with IC2 part 2  $Q_{\rm D}$  output. The output of this second section of IC3 is fed back to the clear input of IC2 part 2. This feedback causes IC2 part 2 outputs to be reset to zero every llth clock cycle (see Figure 3.4). The  $Q_{\rm C}$  output of IC2 part 2, i.e. 1745Hz, is passed to IC8 DO input.

IC8 output, to the RS232 interface, is selected by the values applied to its A, B and C inputs. These inputs are taken from the setting of the RS232 baud rate switch Sl.

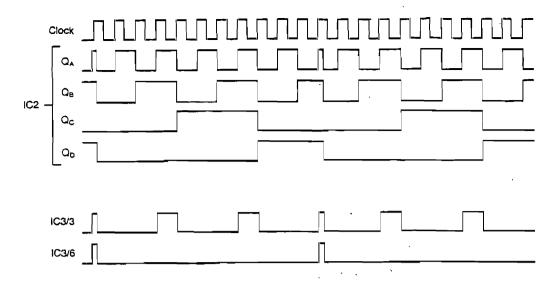


Figure 3.4 I/O Clock Timing

#### 3.8 RESET (Sheet 1)

The microprocessor reset circuit consists of binary counter IC5 and its associated components.

When there is no power loss to the instrument, i.e. PWDN- is at logic 1, IC5 is enabled to count, clocked by the 37.5Hz signal from the I/O Clock circuit. On the tenth count IC5  $Q_{\rm A}$  output will rise to logic 1 and enable a Reset pulse to the microprocessor set via IC6 pin 3. However, under normal operating conditions the microprocessor (IC401 on board 4) periodically clears IC5 by addressing \$4C00 to disable the count. If the microprocessor does not address \$4C00 for approximately 130 to 160 milliseconds, reset is enabled.

When a power down occurs, the microprocessor must have sufficient time to run a checksum of its memory contents, etc, before it receives a reset command. The PWDN- signal is therefore applied to capacitor C2 and whilst this capacitor charges up 'Reset-' is held off. The time constant set by C2 and R4 allows sufficient time for the microprocessor to save its memory contents.

If Reset is disabled at switch Sl, the microprocessor will not be reset regardless of the state of the power fail input.

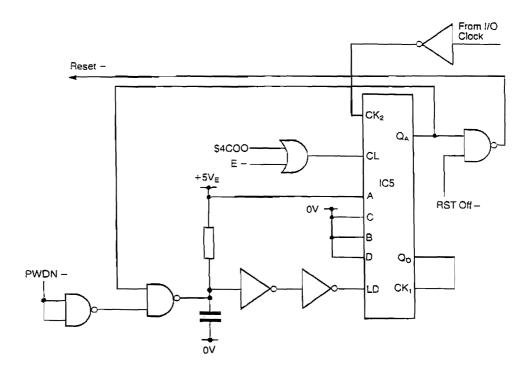


Figure 3.5 Reset Control

#### 3.9 POWER SUPPLIES (Sheet 2)

The instrument is fitted with a multi-purpose mains input unit mounted on the rear panel. This contains the mains input socket, fuses, voltage selector and filter. Switches a to e set the voltage to be supplied to transformer Tl.

#### 3.9.1 Earthy Power Supply

The earthy power supply generates ±12V, +5V and +40Vdc for the earthy circuits, and includes a power fail detect circuit.

#### ±12V Supply

The ac voltage is applied, via PL52, to bridge rectifier D54 where it is full-wave rectified. The rectified output is smoothed by capacitors C59 and C60, and passed through resistors R73 and R74. Zener diodes D60 and D61 finally drop the voltage level down to  $\pm 12$ V.

#### +40V Supply

The ac voltage from PL52 is passed to bridge rectifier D55 via voltage doubling capacitors C56 and C57. The rectified output is smoothed by C58 and applied to 5V regulator IC52. The 30V zener diode D56, between the +5V rail and the G input of IC52, supplies +35V. The +5V added to this by IC52 gives the +40V required. C61 provides high frequency stability.

#### +5V Supply

The +24V unregulated output from D54 is applied to the +5V circuit at TR54. Refer to the simplified diagram in Figure 3.6.

When TR54 is closed, it is in saturation at a voltage drop of approximately lV. When TR54 is opened L52 drives its left-hand end negative until diode D57 latches in and conducts; initially at the same instantaneous current that had been flowing in TR54 just prior to its opening. The voltage at point (A) is approximately equal to  $V_{\rm in}$  for the time TR54 is closed ( $T_{\rm on}$ ) and approximately equal to 0V for the time TR54 is open (T-Ton). The filter L52, C67 averages out the peak-to-peak ripple voltage of  $V_{\rm in}$  and produces at  $V_{\rm O}$ , a constant dc output voltage whose value is given by:

$$V_0 = Vin \frac{(Ton)}{T}$$

Output voltage Vo is regulated by controlling the ratio of Ton/T. The frequency T is fixed and  $T_{\rm OR}$ , the duration of the "on" time for TR54, is varied by pulse width modulator IC55, turn-on pulse amplifier TR56, TR53 and associated components.

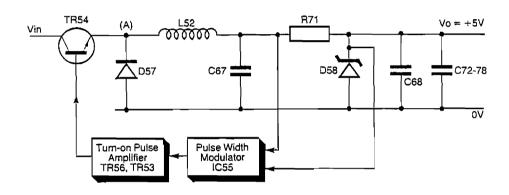


Figure 3.6 +5V Supply Simplified Diagram

Zener diode D58 provides over-voltage protection, capacitor C68 removes voltage spikes and capacitors C72 to C78 provide local high frequency decoupling. R71 provides a current limit of about 2A via IC55.

#### 3.9.2 Power Fail Detect

IC56, D59 and associated components provide a power fail detect circuit the output of which is applied to the reset circuit on Sheet 1.

When the output from capacitor C59 falls to less than +21V the ouput of comparator IC56 falls to the negative rail value. This makes PWDN- equal to logic 0.

#### 3.9.3 Floating Power Supply

The ac voltage from PL51 is applied to bridge rectifier D51. There it is full-wave rectified and smoothed by C51 before being applied to transistor TR52.

When TR52 is closed, it is in saturation at a voltage drop of approximately lV. When TR52 opens L51 drives its left-hand end negative until D52 latches in and conducts. The voltage at point (B) is therefore approximately equal to  $V_{\rm in}$  during the time TR52 is closed (Ton) and approximately equal to lV0V during the time TR52 is open (T-Ton). Filter L51, C55 averages out the peak-to-peak ripple voltage of lV1 and produces at lV2, a constant lV3 output voltage given by

$$V_o = Vin \frac{(Ton)}{T}$$

Output voltage Vo is regulated by controlling Ton, the duration of the 'on' time of TR52, via Pulse Width Modulator IC51, Turn-on Pulse Amplifier TR55, TR51 and associated components.

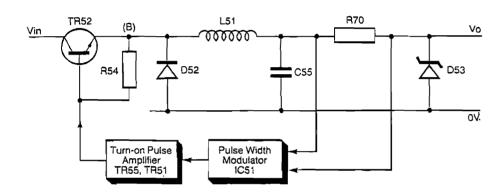


Figure 3.7 Floating Power Supply Simplified Diagram

Zener diode D53 provides overvoltage protection and R70 gives a current limit of about 2A.

A Vo value of  $+5V_{\rm D}$  is output to board 5 via SK51.  $+5V_{\rm S}$  is output to provide voltage sensing. The signal is returned to the circuit and compared with the reference value supplied to IC51.

SK51 also outputs 31V and 17V ac for use on board 5 the 'floating power supply circuit.

#### 3.10

TEST POINTS
The following Test Points are provided to assist in printed circuit board fault-finding.

Table 3.5 Test Points

Test Point (TP)	Signal
1 2 2	TR52 Drain OV
3 <u>.</u>	BLEEPER +
4	BLEEPER -
5	Bl -
6	Bl +
51	IC55 CT input
52 53	IC51 CT input OVE
54	+5VD
55	OVF
56	+12V
57	0VE

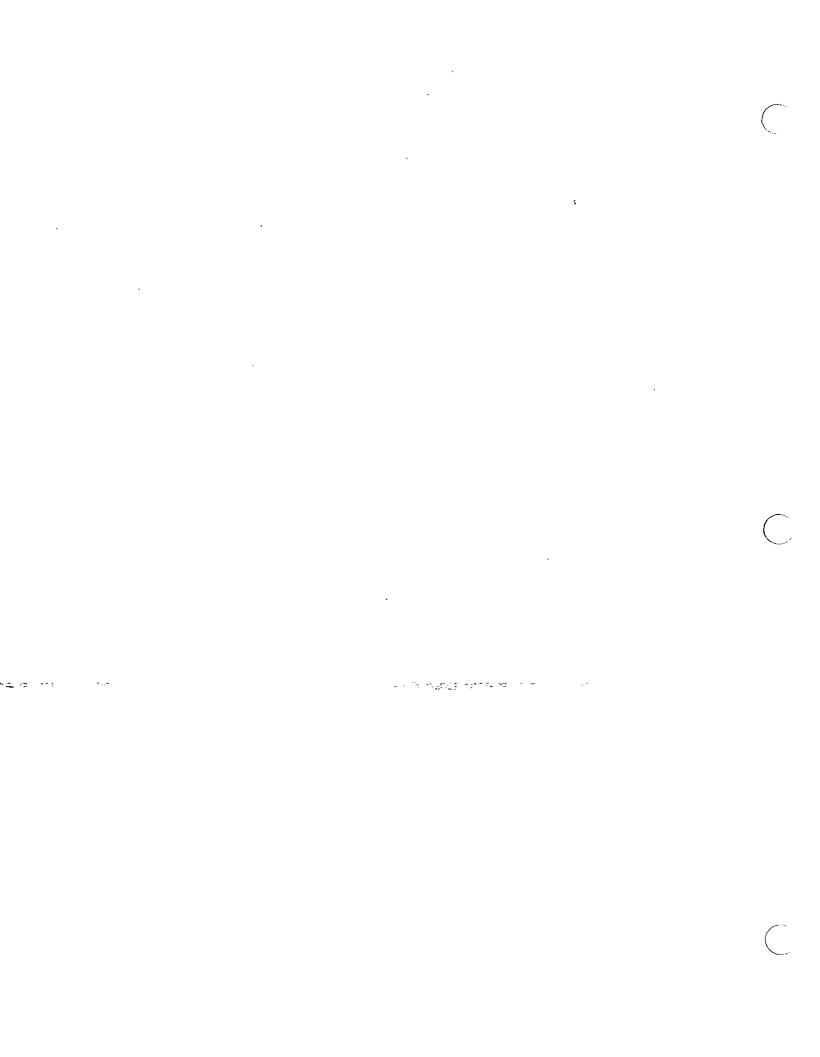
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# CHAPTER 4

# Printed Circuit Board 14

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#### 4.1 MICROPROCESSOR SET

This circuit controls the other logic boards and consists of a microprocessor IC401, read only memory (ROM) IC412 to 415 and IC430, and random access memory (RAM) IC406 to 411.

IC401 contains all the functions required for multi-instruction processing; an arithmetic and logic unit; instruction decode and address registers; an instruction register; all of the clock and logic circuits required for timing and a full complement of data bus lines.

The microprocessor can modify its sequence of addresses on the basis of the results of previous operations. It can also store its own state when interrupted (IRQ) and continue from where it left off, when the Interrupt cycle is satisfied.

# 4.1.1 Read/write $(R/\overline{W})$

This signal determines the direction of data\_flow between the microprocessor and its peripherals. When R/W is at logic 1, Read is selected; when at logic 0, Write is operative.

#### 4.1.2 Interrupt Request (IRQ)

Several of the 7081 and 7071 internal and interface interrupt signals (DMA INT-, RS232 INT-, GP-IB INT- etc.) are combined in IC13 on printed circuit board 3 to form an Interrupt signal to the microprocessor. A logic 0 IRQ- from IC13 causes the microprocessor to initiate the interrupt sequence which begins with the microprocessor, after finishing its current instruction, testing the Interrupt Mask in the Condition Code Register and storing the contents of its programmable registers in memory locations specified by the Stack Pointer.

IC13 outputs a unique set of values on its A, B and C outputs, dependent upon which of the interrupts has been generated, to IC15 which buffers the signals and passes them onto the data bus. The microprocessor reads these signals from the data bus and thereby knows which interrupt requires service.

When the interrupt has been serviced, the microprocessor carries on from where it stopped.

## 4.1.3 Non-Maskable Interrupt (NMI)

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The Non-Maskable Interrupt (NMI) is recognised by the microprocessor as soon as the NMI- line goes to logic zero. The interrupt is used as a power-failure sensor.

Except for the fact that it cannot be masked, the NMI interrupt sequence is similar to IRQ. After completing its current instruction, the microprocessor stacks its registers, sets the Interrupt Mask and fetches the starting address of the NMI interrupt service routine.

#### 4.1.4 Reset (RESET-)

The Reset interrupt is used following power on to reach an initialising program that sets up system starting conditions. Therefore, the RESET- sequence is initiated by a positive going edge. Also, since it is normally used only in start-up mode, there is no reason to save the microprocessor contents on the stack.

#### 4.1.5 Address Bus and Data Bus

The 16 line (A0 to A15) address bus controls data transfer between the microprocessor set, input/output interfaces, memories etc. The transference of data can take place over part of, or the whole of the 8 data lines of the data bus (D0 to D7).

#### 4.2 ADDRESS DECODERS

The Address Decode circuit provides enable signals for the rest of the circuitry on this printed circuit board and consists of decoders IC416, 417 and 418, 2-to-1 Selector IC419 and associated components.

IC416 uses address lines Al3, Al4 and Al5 to generate logic 0 enable signals to the ROM and address decoder IC417. Refer to Table 4.1.

Address Lines IC416 Output Signals \$C000 \$A000 \$6000 \$E000 \$8000 \$4000 A13 A14 A15 (IC412) (IC413) (IC414) (IC415) (IC430) (IC417)Ω O ì 

Table 4.1 IC416 Operation

IC417 is enabled by a logic 0, \$4000 signal from IC416 to produce logic 0 signals, from address lines AlO to Al2, to PL401, IC419, IC420 and the DMA, IC402. Refer to Table 4.2.

Table 4.2 IC417 Operation

Address Lines				IC417 Output Signals						
-A10	All	A12	\$5C00 (PL401, 40)	\$5800 (PL401, 39)	\$5400 (PL401, 33)	\$5000 (IC419, 13,11)	\$4C00 (PL401, 37)	\$4800 (PL401, 36)	\$4400 (IC420, 8)	DMA SELECT (IC402,2)
0 1 0 1 0 1 0 1	0 0 1 0 0 1 1	0 0 0 0 1 1 1	1 1 1 1 1 1 0	1 1 1 1 1 1 0	1 1 1 1 0 1	1 1 0 1 1 1 1	1 1 0 1 1 1	1 0 1 1 1 1	1 0 1 1 1 1	0 1 1 1 1 1 1

IC418 is enabled by the A14 and A15 signals from the address bus, i.e. as long as both these signals are the same, IC418 uses address lines A11, A12 and A13 to provide enable signals to the RAM. Refer to Table 4.3.

Table 4.3 IC418 Operation

	Add	ress	Lines		IC418 Output Signals					
All	A12	A13	A14	A15	\$2800 (IC411)	\$2000 (IC410)	\$1800 (IC409)	\$1000 (IC408)	\$0800 (IC407)	\$0000 (IC406)
0 1 0 1 0 1 0 1 x x	0 0 1 1 0 0 1 1 1 X	0 0 0 1 1 1 1 1 X	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1 0	l l l l l l l Disab	led	1 1 0 1 1 1	1 0 1 1 1 1	1 1 1 1 1	0 1 1 1 1 1 1 1 1

The inputs to IC418, are also dependent upon links LK3 to LK8, which are, in turn, dependent upon the RAM fitted. Refer to Table 4.4.

Table 4.4 Links LK3 to LK8

RAM Fitted	Links Made					
. RAM FILLED	LK3	LK4	LK5	LK6	LK7	LK8
TC5516P or HM6117P	✓	-	✓	_	✓	
HM6116P HM6264	<b>√</b> -	<i>-</i> ✓	<b>√</b>	 ✓	<b>√</b>	- ✓

If HM6264 RAMs are fitted, the only enable signals generated by IC418 are \$0000 and \$2000.

IC419 is enabled by the  $R/\overline{W}$  signal from the microprocessor; a Read signal selects the IC419 B inputs for output and a Write signal selects the A inputs. The lA, 2B, 3A and 4A inputs of IC419 are held to logic 1, the lB and 2A inputs to logic 0 and the 3B and 4B inputs are supplied by the \$5000 signal from IC417. Refer to Table 4.5.

Table 4.5 IC419 Outputs

Inp	ıts	IC416 Output Signals					
Select	\$5000	ly(RD)	2Y(WR)	3Y(R\$5000)	4Y(W\$5000)		
1 0 0	1 0 1 0	0 0 1 1	1 1 0 0	1 0 1 1	1 1 1 0		

The  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  outputs from IC419 are applied to the GP-IB Interface and the RAM. The R\$5000 and W\$5000 signals are fed off the printed circuit board via PL401 pins 35 and 34 respectively.

- 4.3 DIRECT MEMORY ACCESS (DMA)
  The DMA procedure used in 7081 and 7071 can be briefly described as follows:-
  - \* The microprocessor, (IC401), loads the DMA controller (IC402) with a starting address for the memory transfer and the number of words to be transferred.
  - \* When the 7081 or 7071 input has data ready to be transferred to the memory or when the output is ready for transfer from the memory, the DMA controller sends a DMA request to the microprocessor.
  - \* The microprocessor acknowledges the DMA request, floats its address and data buses and appropriate control lines, and suspends any processing that requires use of the address and data bus.
  - \* The DMA controller provides an address to memory and control strobes to read or write memory. The input/output provides or accepts the data on the data bus. After a data byte is transferred, the DMA controller increments its address register and decrements its word count register. If the required number of words has not been transferred, the DMA controller repeats this step when the input/output is ready with the next data word.
  - \* When the required number of words has been transferred, the DMA controller terminates the DMA request and interrupts the microprocessor to indicate that the DMA transfer is complete.

The DMA interface consists of a 16-bit address bus, an 8-bit bidirectional data bus and the following control signals; BA+ or DMA GRANT, BREQ- or DMA REQUEST- and R/W.

The BREQ- (DMA Request) signal from the DMA circuitry commands the microprocessor to halt by going low. The Bus Available (BA+) signal from the microprocessor goes to a logic 1 when the microprocessor has halted and all three-state lines are in the high impedance state. The R/W line is a command signal from the DMA channel to control the direction of transfer through the DMA interface. For the system to operate correctly, the DMA circuitry connected to the microprocessor's address bus, data bus and R/W line must have three-state outputs which are in the high impedance state when BA+ is low and the microprocessor is controlling the address, data and control buses. The time from the BREQ- line going low to the microprocessor halting and producing a BA+ (DMA Grant) will be variable depending on what instruction is being executed at the time BREQ- goes low and in which cycle of that instruction BREQ- goes low.

DMA requests involve two byte transfers; the first transfer has address line AO low (even address) and the second AO high (odd address). Before and after each transfer, the DMA performs a dummy cycle.

There are two channels which make requests to the DMA; Channel 0, the Display, and Channel 1, the Floating to Earthy Data Link.

#### 4.3.1 Channel 0

Channel 0 requests are clocked by the 4800Hz signal from the I/O Clock circuit on printed circuit board 3. Twenty-four requests are made before the circuit generates an interrupt.

Once the DMA has the bus for a Channel O transfer, a dummy cycle occurs followed by the first DMA Transfer. When the transfer begins, Transfer Strobe - (TSTB-), Valid Memory Address - (VMA-) and Transfer Request O (TRQO+) fall to logic low, and, during the transfer, Even Data Strobe - (EDATSTB-) goes low to the Display for half an E clock cycle.

The DMA then performs two dummy cycles followed by the second transfer. During this-second transfer Odd Data Strobe - (ODATSTB) goes low to the Display for half on E clock cycle.

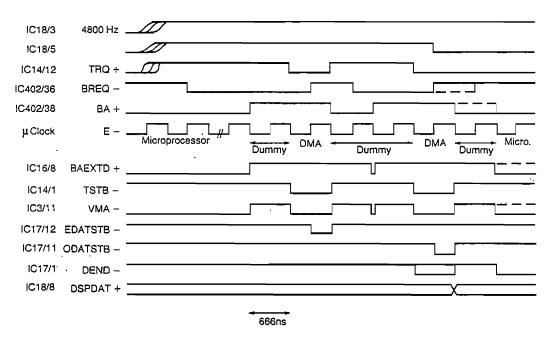
DSPDAT+ goes high on the rising edge of the 24th Odd Data Strobeand goes low on the rising edge of the next.

Refer to Figure 4.1 for the DMA timing for this channel.

# 4.3.2 Channel 1 Channel 1 requests, via the Data Received (DR) line from IC9 pin 19 on printed circuit board 2, are delayed in IC29 by five E clock cycles. If a Channel 0 request occurs during this delay, Channel 0 takes the DMA, as it has a higher priority than Channel 1, and clears IC29. Once Channel 0 has finished its transfer, the Channel 1 request appears at the DMA after a further five clock cycles. This delay circuitry prevents latch up occuring

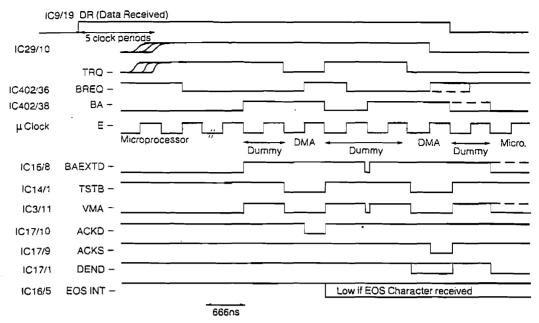
between the earthy and floating processors.

Channel l transfers are similar to Channel 0 transfers except that Acknowledge Data - (ACKD-) goes low during the first transfer (instead of EDATSTB-) and Acknowledge Status - (ACKS-) goes low during the second transfer (instead of ODATSTB-).



The dotted lines show the Channel 0 Data Chain cycle TAKA = 0 during this cycle, DSPDAT + goes high and low on the next cycle.

Figure 4.1 DMA Timing - Display (Channel 0)



The dotted lines show the Channel 0 Data Chain cycle TAKA = 1 during the time that TSTB - is low.

Figure 4.2 DMA Timing - Receive Floating Data (Channel 1)

If an End of String (EOS) character (ASCII 8D) is received during a DMA cycle, an EOS Interrupt is generated, i.e. EOS INT - goes low. The software services this interrupt and resets the DMA channel.

A DMA FL Interrupt is generated if more data comes in than expected or, if a negative acknowledge is received from the floating side.

Refer to Figure 4.2 for the DMA timing for this channel.

In order to exit from the DMA mode, the BREQ- line is switched high (synchronously with the clock), the BA+ signal returns low and the microprocessor resumes control of the bus. When BA+ falls low, the DMA channels address, R/W and data line are in the high impedance state.

#### 4.4 GP-IB INTERFACE

The GP-IB Interface (IC420), with its associated bus-drivers, provides a means of connecting the voltmeter's microprocessor with external devices connected to the IEEE Standard bus. The handshake lines DAV, NRFD, NDAC are handled automatically by IC420.

Essentially the GP-IB Interface comprises fifteen registers, (one, the Address Switch Register IC424, is external to IC420). Seven of the registers may be written to by the microprocessor depending on the state of control lines RD, WR and RSO to RS2.

## 4.4.1 GP-IB Address Selection

The voltmeter address and Talk/Listen Status are set up on switch SW801 on printed circuit board 8. The values of the switch settings are then passed via socket SK801 to SK414 on printed circuit board 4 and from there via non-inverting line drivers IC424, to the data bus.

IC424 is enabled by a logic 0 \$5800 signal from IC417 in the Address Decode circuit.

#### 4.4.2 GP-IB Signal Lines

The microprocessor/GP-IB Interface and GP-IB Interface/IEEE bus signal lines shown in Figure 4.3 are summarised below:

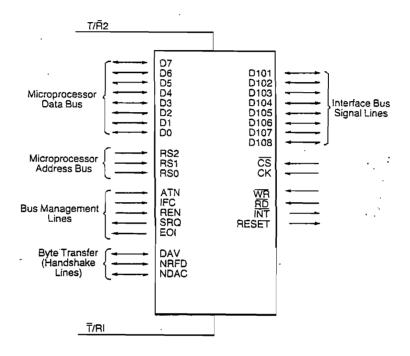


Fig. 4.3 GP-IB Interface Signal Lines

Bidirectional Data (D0-D7) These lines allow data transfer between the microprocessor and the GP-IB. The data bus output drivers are three-state devices that remain in a high impedance (off) state except when the microprocessor performs a GP-IB read operation.

Chip Select  $(\overline{\text{CS}})$  IC417 selects the GP-IB interface by pulling the line low.

RD, WR These signals are generated by the microprocessor to control register access and the direction of data transfer on the data bus. In conjunction with control lines RSO to RS2 (see below), the RD line, when low, selects one of the eight read only registers; when WR is low one of the seven write only registers is selected.

Register Select (RSO, RS1, RS2). Used in combination with  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  for register selection.

Interrupt (INT) The INT output goes to the common interrupt bus for the microprocessor. The INT line is set active (low) when an interrupt occurs, and remains so until the microprocessor reads the Interrupt Status register.

Reset The active high Reset line is used to initialise IC420 during power-on/initialise. Reset is driven by an external power-up reset circuit.

Bus Management Lines (ATN, IFC, REN, SRQ, EOI) These lines are used to manage an orderly flow of information across the interface lines.

Attention (ATN) is sent by a controller over the interface. During the ATN active state, devices monitor the data lines (D0 to D7) for addressing or an interface command.

Interface Clear (IFC) This signal is used to put the interface system into a known quiescent state.

Remote Enable (REN) is used to select one of two alternate sources of device programming data: local or remote control.

Service Request (SRQ) When active, the signal indicates the need for attention in addition to requesting an interrupt in the current sequence of events. This indicates to the controller that a device on the bus is in need of service.

End or Identify (EOI) signals the end of a multiple byte transfer signal and, in conjunction with ATN, executes a parallel polling sequence.

Clock Input (CK) Derived from the microprocessor clock generator, this input is used to synchronise control and data transfer throughout the interface.

Signal Lines (DIO1 to DIO8) These bidirectional lines allow for the flow of eight-bit ASCII interface messages and device dependent messages.

Byte Transfer Lines (NDAC, NRFD, DAV) These lines allow for the proper transfer of each data byte on the bus between talkers and listeners. NRFD is high to indicate that all listeners are "ready for data". A talker indicates that "data is valid" by putting DAV low and the transfer begins when NRFD falls low. Upon the reception of valid data by all listeners, NDAC goes high indicating that the "data has been accepted" by all listeners.

Transmit/Receive Control Signals  $(\overline{T}/Rl)$  and  $\overline{T}/R2$ ) These two signals control IC421 and 422 which drive the interface bus. The transmit/receive inputs of REN, IFC and ATN are held high to receive, while SRQ is held low to transmit. EOI (transmit or receive) is controlled by  $\overline{T}/R2$ .

## 4.5 TEST POINTS

The following Test Points are provided to assist in printed circuit board fault finding.

Table 4.6 Test Points

Test Point (TP)	Signal
1 2 3 4 5 6 7 8	START STOP CLOCK E GND A15 OVE Not connected +5V

(TP1, 2, 3 and 5 are used with Locator).

# CHAPTER 5

# Printed Circuit Board 5

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#### 5.1 INTRODUCTION

Board 5 contains the voltage-to-time converter, the glug counters, the microprocessor and the non-volatile memory (NVM). It also provides a clock divider and oscillator circuit, and the reference, ratio and ohms circuits for the instrument. The board has its own power supply. A schematic of these functions with their interconnections is shown in Figure 5.1.

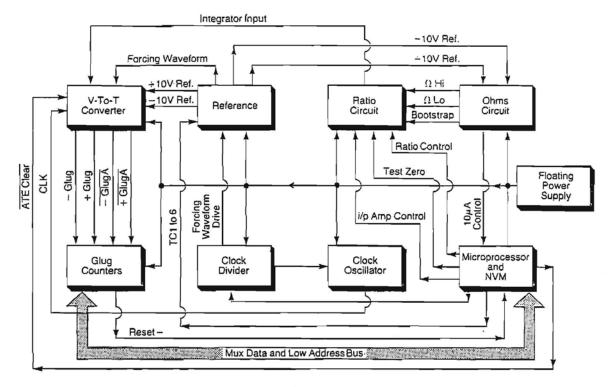


Figure 5.1 Board 5 schematic

#### 5.2 VOLTAGE-TO-TIME CONVERTER (Sheet 1)

This circuit, comprising an integrator, comparators, clock synchronised bi-stables and reference switching FETs/transistors, converts the voltage output from the main amplifier into two pulse trains. The pulses are used to gate the clock into a reversible counter which produces a nett count proportional to the measured input.

The integrator, which comprises IC201 (a d.c part) and IC202 (a conventional fast part) has the following inputs connected:

- 1. The input to be measured
- 2. The forcing waveform
- 3. +Reference, -Reference or OV.

With the input at OV, and a 160Hz forcing square wave applied continuously to the integrator, the output is driven alternatively positive and negative through the thresholds of the two comparators IC203 and IC204. The state of the two comparators is followed by IC205, which synchronises the transitions to the clock. Outputs from IC205 are then used to drive FETs TR201 to

TR204, TR207, TR208 and transistors TR205, TR206, which switch the reference voltages or 0V to the integrator input. With this arrangement the output will always remain dynamically balanced about zero, irrespective of the input to the integrator.

The ratio of R202 to R201 is set so that, without calibration, the instrument is guaranteed to read high and a calibration constant of <1 is required. This ensures that there are no missing digitised codes.

#### 5.3 REFERENCE VOLTAGE (Sheet 2)

The reference voltage (+10V, -10V) is generated from D301 by IC305 and scaling resistors R306 a to d. IC306 and R305 determine the zero of the V-to-T convertor as they are used to center the reference voltage.

IC307 switches between +10V and -10V to generate the forcing waveform. R310 and R311 reduce transients (due to this switching) on the reference voltage.

R308 and R309 current limit the reference output in the event of a short-circuit. D302 ensures that, at power-up, the reference circuit starts-up in the correct direction. (The reference circuit has two stable operating states.)

The remainder of the circuit is concerned with

- (a) setting up the linear component of the temperature coefficient of D301 and
- (b) compensating for the curved component of the temperature coefficient of D301.

The linear component is controlled by IC301, which is a D-to-A convertor, and IC304, which is a buffer. The digital signals present on TCl to TC6 control the output current of IC301 and thus the output voltage of IC304, which may swing between 0V and -10V. This in turn varies the current through D301 and hence varies the linear temperature coefficient. R303 converts the output swing of 0V to -10V into a current swing through the diode.

The curved component of the temperature coefficient is compensated for by D351, IC351 and associated components.

D351 generates a current proportional to absolute temperature of  $l\mu A/K$ . This is offset by a current through R351 such that, at 27°C (300K), the voltage at pin 2 of IC351A is approximately zero. As a result, IC351B output will also be at zero, since it has no input, and transistor IC352 pins 3,4,5 will be biased off.

When the temperature is less than 27°C, IC351A pin 2 goes negative. This produces a positive output, which is fed back via D352. Hence IC351A acts as a virtual earth amplifier with an input of luA for every degree Centigrade below 27°C.

The ratio of R352 to R353 (6.8k:10k) causes a positive current to flow into IC351B virtual earth, and an equal current of  $+0.6\mu A/^{\circ}C$  to flow through transistors IC352 pins 1.2,3,9,10 and 11.

The action of IC352 is similar to that of the rms convertor and the output current from IC352 pin 5 is (Iin)2/Iref where Iref is the current supplied by R354. Hence a square law relationship is established between the output current and the input current.

When the temperature is greater than 27°C, IC351A pin 2 goes positive. This produces a negative output, which is blocked by D352. Hence, the voltage at IC351A pin 2 (source impedance 33k-R351) is developed across the load of R352 and R353 in series. The current at IC351B pin 6 (virtual earth) is again  $0.6\mu\text{A}/^{\circ}\text{C}$  and causes an equal current to flow through IC352 pins 1,2,3,9,10 and 11.

The result is that for all temperatures a positive current of  $0.6\mu\text{A}/^{\circ}\text{C}$  flows into IC351B virtual earth, i.e. IC351A effectively performs the function of the absoluter in the AC RMS converter.

The output current from IC352 pin 5 is therefore:

$$\frac{[(T-27)x0.6]_2}{I \text{ ref}}$$
 µA

where T is the temperature in degrees Centigrade.

The output current is developed across R355, so that it is added to the zener voltage. This is because the diode characteristic is such that on either side of 27°C, the voltage falls.

#### 5.4 RATIO CIRCUIT (Sheet 3)

Ratio measurements are performed using Hi and Lo lines. The voltages are switched through their own amplifier to avoid difficult switching of the main input amplifer. The ratio signals are routed into the main system just before the integrator.

TR502 buffers the input and generates bootstrapped rails to power the main amplifier IC502. TR504 protects IC503 against over voltage during negative measurements.

Switching allows either the ratio output, the input amplifier output, or zero to be measured. Zero is used during a drift correct or self-test. Transistors TR505 and TR506 are used to switch the signals as long as the input or output lies in the range -15 V < V < +15 V.

To prevent variation of resistance at turn-on, transistors TR505, TR506, TR508, TR509, TR516 and TR517 must be turned on by a voltage which has a fixed value above the signal voltage. This is supplied by the input signal 'I/p AMP + 5V BOOTSTRAP'. If this is not the case, non-linearity occurs as the input impedance to the integrator is only  $160 \mathrm{k}\Omega$ .

Relay RLl isolates the current source terminals from the current sources in non-kohm modes, when a two-wire cable is being used and RL50l connects the  $10\mu A$  current source straight into the integrator for the kohm self-test facility.

#### 5.5 OHMS CIRCUIT (Sheet 4)

True four-terminal ohms measurements are made since the current source is floating with an independent power supply. The reference is transferred across to the independent supply using IC601, IC602 and optocouplers IC605 a and b to give isolation. The only currents which flow between the two sections are insulation leakage currents and amplifier bias currents (~10pA).

The reference is generated across R604. This provides a current which regenerates a voltage across R609. This is then applied across either R611 or R612 to create either  $10\mu\text{A}$  or 1mA. FET switching is employed and hence a separate current switch and voltage sense FET is required for each position.

D608 ensures that the voltage dropped across TR607 and TR609 does not forward bias the gate-source junction and D605, D609, D610 are protection diodes in the event of a mains voltage being inadvertantly applied to the terminals.

In some cases the reference voltages collapse briefly after power-up and this can inject current into pin 10 of IC601 and IC602 via capacitors C605 and C606. R616 and R617 limit this current to a value which does not cause latch-up.

Since the power rails are assymetrical about OV and only one transformer winding is used, D615 is included in the circuit to improve the balance and equalise the voltage stress on IC607 and IC608.

This circuit is used for measuring resistances up to  $1M\Omega$ . Above this value a conductance method is used, ratio-ing the unknown resistor to the  $9.9M\Omega$  attenuator resistor. The switching for this is done in the input attenuator.

## 5.6 GLUG COUNTERS (Sheet 5)

The outputs from the V-to-T converter -GLUGA, +GLUGA, +GLUG and -GLUG are used to gate clock into a reversible counter chain comprising IC812, IC807, IC810 and IC811.

If the output of NOR-gate IC822 pin 10 rises to logic high, the counters are inhibited.

The  $\overline{\mathbb{Q}}$  output of D flip-flop IC835 determines the direction of the count; if  $\mathbb{Q}$  goes low, the counters count up, if  $\mathbb{Q}$  goes high, the counters count down. As the D and Clock inputs to IC835 are permanently tied to  $V_{EE}$ , the state of the  $\mathbb{Q}$  output is solely dependent upon the state of the Reset and Clear inputs, i.e. —GLUGA and +GLUGA respectively. If —GLUGA goes low, the  $\overline{\mathbb{Q}}$  output also goes low and conversely, if +GLUGA goes low, the  $\overline{\mathbb{Q}}$  output goes high.

+GLUGA and -GLUGA are derived from the Q outputs of IC205 b and d in the V-to-T converter. IC205 b has comparator IC203 output applied to its D input and IC205d has comparator IC204 output applied to its D input. Both flip-flops are clocked by the 5.24MHz clock signal from IC835 in the clock oscillator circuit. Figure 5.2 shows the timing of +GLUGA and -GLUGA generation and the operation of the counter enable direction pulses.

The Q output of IC205b is applied to the D input of IC205a which outputs +GLUG on the next rising clock edge to IC821 pin 10 and IC822 pin 8.

IC821 gates together +GLUG and  $\overline{\text{+GLUGA}}$  to  $\overline{\text{supply}}$  the 'clear' signal for IC813. Clear is generated when both +GLUGA and +GLUG are logic high.

The  $\overline{Q}$  output from IC205d is also applied to the D input of IC205c which outputs -GLUG on the next rising clock edge to IC822 pin 9. IC822 provides 'chip enable' for IC812 as previously described.

IC813 acts as a glug synchronisation monostable and is continuously triggered until the final count down pulse, when the  $Q_{\rm B}$  output (pin 13) goes low. Latches IC809 and IC808 then record the contents of the counters. After 0.5 $\mu s$ , IC813 triggers to reload the counters with zero and to send an interrupt request (IRQ-) to the microprocessor IC801. The microprocessor then reads the contents of the two latches (by sending GLUG HI-and GLUG LO- via IC805) and also re-enables IC813 in readiness for the next glug input.

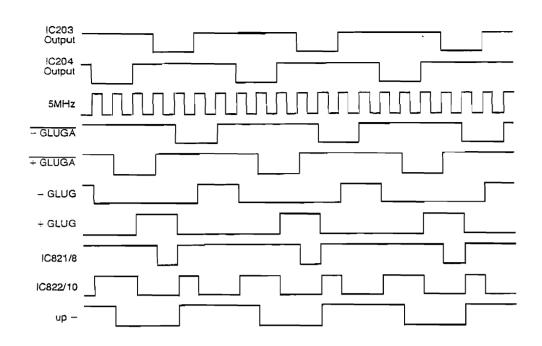


Figure 5.2 Glug Generation and Timing

5.7 CLOCK DIVIDER (Sheet 5)
A mains derived 17VAC signal is buffered and isolated by IC303
before being applied to IC834. The output from IC834 pin 6 is
applied to the microprocessor IC801 pin 19, which measures the
mains frequency and sets its 400Hz, 60Hz lines accordingly. Refer
to Table 5.1.

Table 5.1 Microprocessor Frequency Settings

	Microprocessor	Output Lines
Mains Frequency	400Hz	60Hz
50Hz 60Hz 400Hz	0 0 1	1 0 1

If the mains frequency is equal to 50Hz, the  $Q_{\rm C}$  output of IC819 is low to IC822 pin 2. IC822 therefore passes the mains frequency (50Hz) to the clock input of IC820. 60Hz is high to the A input enabling IC820 to divide the input frequency by 5 to give 10Hz at its  $Q_{\rm B}$  output. If the mains frequency is 60Hz, 60Hz is low and IC820 divides the input by 6 to give 10Hz at  $Q_{\rm B}$ . With a 400Hz mains frequency, the top half of IC819 is enabled giving 400  $\div$  8, ie 50Hz, at its  $Q_{\rm C}$  output. IC822 is disabled at pin 6 but enabled at pin 2 to pass this 50Hz signal to IC820 pin 2. IC820 then divides the frequency by 5 to give 10Hz at its  $Q_{\rm B}$  output.

The bottom half of IC819 is driven by IC814 and IC815. IC814 is clocked by the 5.24MHz signal from the clock oscillator circuit. The 5.24MHz signal is repeatedly divided down by IC814 and IC815 until 160Hz is output to IC819 clock input. IC819 divides this clock by 16 to give the 10Hz signal for IC824.

The forcing waveform drive signal for the reference circuit is also derived from IC814 and IC815. The  $\rm Q_{\bar A}$  (640Hz) and  $\rm Q_{\bar C}$  (160Hz) signals from IC815 are applied to the D3. D1, D2 and D0 inputs respectively of IC833. When IC833 receives a logic high FWS signal from IC830, it outputs 640Hz at Y0 to the reference circuit. (The 640Hz signal is used when the unit is configured for nines = 3). If FWS is at logic low, IC833 outputs 160Hz to the reference circuit.

- The mean dc level on C814 controls the varactor diodes D808 and D809, the capacitance of which determines the frequency of the LC oscillator (TR805, L801 etc.) The output from the clock oscillator is applied via TR806 and TR807 to IC835 which divides the frequency by two to give a clock output. This is divided by 524288 (2<sup>19</sup>) to give the 10HzC signal from IC819/818. The 10HzC signal is phase-locked to the 10Hz derived from the mains input. Thus, the clock oscillator outputs approximately 5.24MHz which varies with the mains frequency.
- 5.9 NON-VOLATILE MEMORY (NVM) (Sheet 5)
  The NVM (IC804) is organised in 1024 x 4 bit nibbles and is accessed via the normal address bus, to specify the NVM address, and the microprocessor (IC801) port 1 (P10 to P15), to specify the function required and to pass data.

The NVM has logical addresses in the range 0 to 1023 and physical addresses in the range 0 to 2046 (even values only). Since the access time of the NVM is slower than the normal microprocessor cycle time, the NVM is addressed twice for each operation. IC805, 823 and 806 convert an even address into the address to be accessed and assert 'chip select'. An odd address causes chip select to be unasserted.

As the NVM holds the calibration data for the instrument, the integrity of the storage is vital. Two data validation measures are used:

- 1. The information is duplicated on two pages.
- 2. Each page has an 8-bit checksum (stored in two consecutive nibbles). Since a simple checksum would not detect an 'all zeroes' failure, the stored checksum is offset by a value held in ROM (IC803). At calibration the information is written into both pages.

At power-up, information is read out of the NVM as a complete page. Page 1 is checked first by the microprocessor (IC801) and, if it is found to be correct, it is transmitted to the 'earthy' processor IC401 on board 4. If page 1 is found to be faulty, page 2 is checked. If page 2 is found to be correct, it is transmitted across: the 'earthy' processor uses this page whilst flagging a non-fatal error condition to the user. If page 2 is also faulty, the 'earthy' processor will use page 2 information whilst flagging a calibration error condition to the user.

An NVM erase voltage is generated by TR804, D806 and associated components, but is present at the NVM only when (i) the NVM is addressed (ii) an even address is applied to IC806, and (iii) Write is enabled. The NVM is not necessarily erased if the Erase voltage is present; erase has to be enabled first.

5.10 FLOATING POWER SUPPLY (Sheet 6)
This circuit produces the floating power for the analogue circuits.

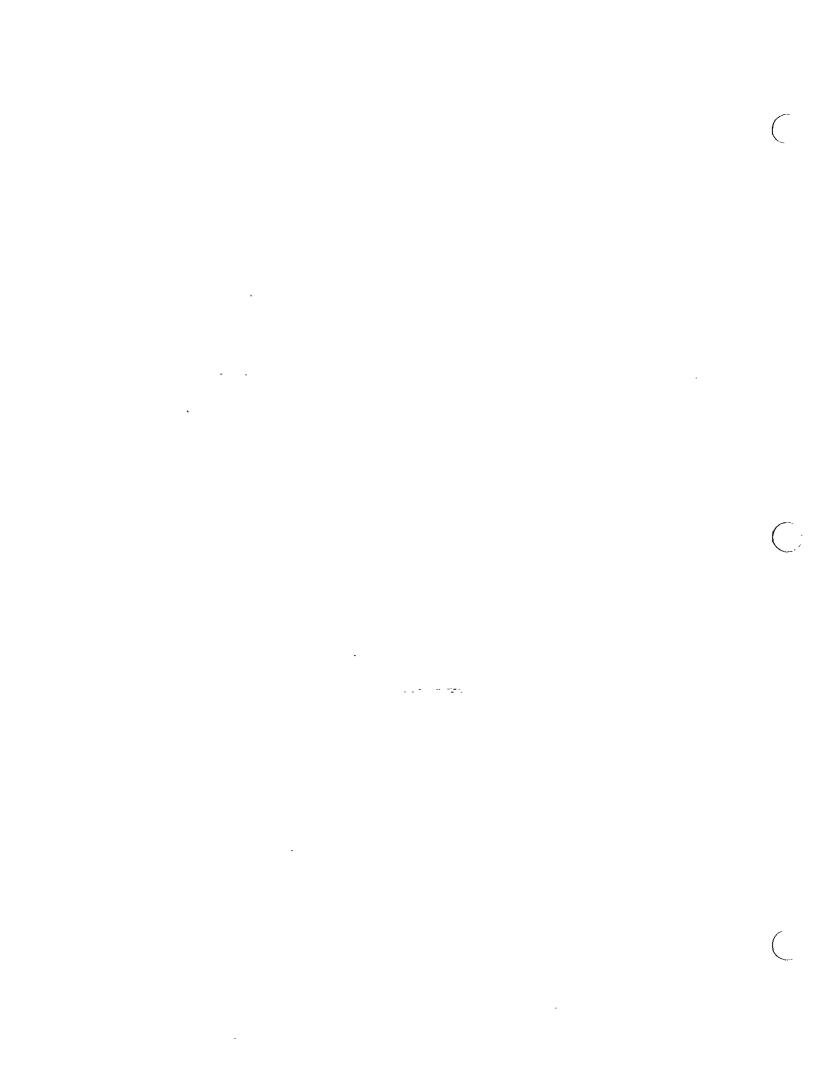
The  $\pm 15V$  supplies are produced from a bridge rectifier circuit, D901 and voltage regulators IC901, IC902. The  $\pm 28V$  supplies are obtained from the same inputs via a voltage doubler and voltage regulators IC903 and IC904.

#### 5.11 TEST POINTS

The following Test Points are provided to assist in printed circuit board fault-finding.

Table 5.2 Test Points

Test Point (TP)	Signal
201 202 203 204 205	Integrator -Glug +Glug Glugs 0V
301	Current
302	10V Ref
303	-10V
304	3.8V
305	0V
501	Ratio In
502	Ratio 6V
503	Ratio -6V
504	Ratio Out
505	OV
601	10V
602	-10V
603	-25V
604	0V
605	22V
606	37V
607	IC604 Input
608	IC604 Output
609	Ohms Control
801	Free S/S
802	Clock
803	GND
804	\$6400
805	-15V
806	\$6500
807	Frequency
901	28V
902	15V
903	0V
904	-15V
905	-10V
906	-28V



# CHAPTER 6

# Printed Circuit Board 6

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#### 6.1 INTRODUCTION

Board 6 contains the input and signal conditioning circuits for the instrument, including the input amplifier, ac attenuator and rms converter. A schematic of these functions, with their interconnections, is shown in Fig 6.1.

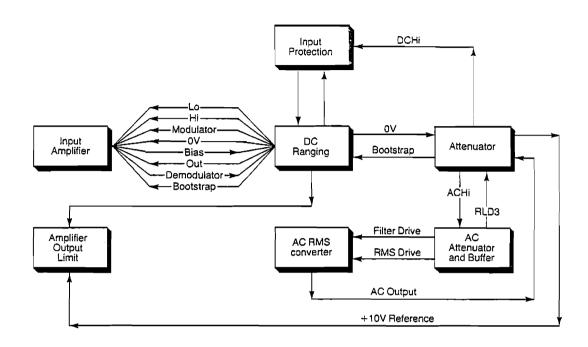


Figure 6.1 Board 6 schematic.

#### 6.2 ATTENUATOR (Sheet 1)

The voltmeter input signals, from either the front or rear panel connector, enter printed circuit board 6 and are fed, via the front/rear switch Sl, through various combinations of relays and resistors, depending upon the measurement function selected. The resistors attenuate the signals to the levels required for the voltmeter's circuitry. Table 6.1 indicates the relays made for different measurement functions.

mable.	6 1	Attenuator	Do lave
Tanie	n	Arremiator	REIAVE

Function	Relays On	
0 to 10V dc	RL5	
10 to 1000Vdc	RL4, RL6	
Vac	RL3	
0 to 1MΩ	RL5	
1MΩ to 1GΩ	RL2, RL5, RL6	
10V Test	RL2, RL4	

Note: RL7 is closed whilst RL5 opens or closes.

AC input signals are passed onto the AC Attenuator and Buffer; dc and resistance signals to the DC Ranging circuit.

#### 6.3 INPUT AMPLIFIER (Sheet 2)

The voltage applied to the amplifier, via the Hi and Lo lines, is limited by diodes D401 and D408 to protect the circuit from accidental overload. The limited voltage is then applied to input FET pair TR401. IC401 is connected to the drains of TR401 to improve the common mode rejection and hence the settling time to transients; if the offset does not change the chopper channel need not resettle.

The output from IC401 is fed directly to IC402 and from IC402 to the amplifier output limit circuitry.

The offset from TR401 is fed, via a filter circuit consisting of R407, R408 and C404, to a bridge modulator made up of four low leakage FETs: TR406, TR407, TR408 and TR409. IC406 provides anti-phase switching signals for the modulator. The amplitude of these signals is determined by diode D404. The resultant modulated signal from the FETs is then amplified by low noise amplifier TR404 and high gain amplifier IC404.

Any dc output is removed by capacitor C410 and the signal is demodulated by IC405 and its associated components.

The amplified offset is fed back into IC401 via R406, which is balanced by R404 to give rejection of rail noise.

IC402 is unity gain stable but TR401 provides gain for its inputs. This extra gain is "lost" by C401 (R402 + R401) in the lower limit and R403 (C401) in the upper limit. The result is to make the combination of TR401 and R403 have a gain of one and no phase shift at high frequencies.

The cross-over frequency between the high frequency amplifier and the chopper channel is approximately 8Hz so that a 6dB per octave roll-off is maintained for most frequencies.

TR412 and IC402 provide low voltages which are defined relative to the input voltage, e.g. -6.2V. These can be used to provide rail currents for TR401 and TR404.

## 6.4 DC RANGING (Sheet 3)

The gain of the main input amplifier is controlled by the scaling resistor network in this circuit. The network also provides an additional measure of input amplifier protection, relative to the bootstrap.

#### 6.4.1 Input Protection

Despite the use of an input attenuator, large input swings could still overdrive the input amplifier. The input protection circuit provides an extra safeguard, limiting the signal line excursions to approximately 15V. The circuit consists of diode Dl01, zener diode Dl02, Dl03 and associated resistors.

#### 6.4.2 Ranging

Resistors Rlll to Rll4 form the feedback paths for the input amplifier. The feedback, and hence the gain, is selected by one of the F.E.T. switches TRlO1 to TRlO3 which are driven from board 5 via the opto-isolators in ICl04.

#### 6.5 AMPLIFIER OUTPUT LIMIT (Sheet 3)

This circuit, which consists of operational amplifiers ICl02, ICl03, diodes Dl07 to Dl14 and associated components, ensures that the input amplifier output does not exceed  $\pm 15V$ . If the output is within these limits, the voltage at the non-inverting inputs to ICl02 and ICl03 is within  $\pm 10V$ . The circuit operation is as follows:

# OV input to ICl02

Amplifier output equals -12V. Dll2 is forward biased, thus enabling the IClO2 feedback loop. IClO3 output equals +12V, but its inverting input is kept at -10V by the reference input. Under these conditions, DlO7 and DlO8 are reversed biased and no current flows to DlO9, DllO, RllO.

#### +10V input to IC102

Amplifier output equals -2V. Dll2 is still forward biased. ICl03 output equals +22V, therefore Dl07 and Dl08 are still reverse biased.

# +15V input to IC102

Amplifier output rises above -2V. Dll2 is reversed biased, thus disabling the feedback loop. The amplifier (ICl02) output therefore rises rapidly in an attempt to equalise its inputs. ICl03 output, on the other hand, continues to track the input  $(V_{\rm in} + 12)$  because of the -10V reference applied to its inverting input. Therefore, as TPl06 rises to the rail voltage and TPl07 equals +27V, diodes Dl07 and Dl08 become forward biased switching Dl09, Dl10, Rl10 onto the input amplifier feedback loop.

#### Large negative voltages input to IC102

D114 in the feedback loop of IC103 becomes reverse biased and forces IC103 output more negative in an attempt to equalise its inputs. IC102, on the other hand, continues to track negative inputs. D107 and D108 are again forward biased and switch D109, D110, R110 into the input amplifier feedback loop.

AC ATTENUATOR AND BUFFER (Sheet 4)
This circuit is required to accommodate either rms ac only or the rms of the ac + dc. For the ac only case, RL701 is closed, RL702 open. For the ac + dc case, both RL701 and RL702 are closed. In any other mode RL702 is closed to keep C701 discharged.

The ac gain of the attenuator is one at RL703 for high frequencies. At low frequencies the gain is rolled off by C701, R703, 707 and 708 in the ac only mode but, in the ac + dc mode, the gain begins to roll off because of C701, R703, 707 and 708 and then, flattens off again at about 0.95 because of R702. Therefore, to give a flat ac + dc response, a similar network, C702, R701 and R704 is introduced into the feedback path of buffer amplifier IC705.

For ac only, the buffer amplifier has a gain of one at all frequencies. In practice, a large capacitor is put in series with TR704 (C703). This gives a slight lift in response at low frequencies to counteract the effect of C701 at frequencies just above the cut-off point.

In the 100mV and 1V ranges, the signal passes through R711 at low frequencies and R722 plus C709 at high frequencies to clamp diodes D712 and D713. The combination of R711 and C709 in parallel, combined with the amplifier input capacitance, gives a gain of about 0.9985.

For the 10V and 100V ranges, the attenuator is put in the  $\div 100$  position and the buffer set to either Xl or Xl0. C706 and C720 compensate for capacitance across R703.

For the 1000V range, the attenuator is put in the  $\pm 1000$  position (R706).

For ac self-test, the attenuator is set to the 1000V position and a square wave generated from the forcing waveform is injected into the bottom of the attenuator. This method of injecting a low signal into the attenuator gives good isolation from the test voltage when normal measurement is being made without adding another relay to the sensitive input amplifier node.

IC705 forms the basis of the buffer amplifier. C704 is included in the circuit to prevent IC705-oscillating in the region of 50Hz. A gain of either 1 or 10 is required from the buffer amplifier, both with a bandwidth of at least 7MHz. TR703 and associated components C714, R721 and R720 provide the gain of 10. They are switched into the feedback loop by IC706, D716, D715, D717 and TR702 acting as a common-base amplifier. IC706 pin 1 is logic low so that D715 is forward biased and D716 causes the cathode of D715 to clamp at -9V. TR702 is an emitter follower which drives the common-base amplifier.

C712 compensates the feedback attenuator for the capacitive loading by the various components connected through TR706 when it is turned on.

To get a gain of one, the output stage is saturated; for this, the bias to TR703 is changed by turning off the low collector output, pin 1, of IC706. As a result, current flows from the positive rail through R705f, g, R716 and R720 (D715 is now reverse biased), and turns TR703 on. This effectively couples the emitter follower TR702 directly to the output. R718 is needed to decouple TR702 from the output load, which is fairly capacitive. Feedback is now unattenuated through TR705, giving an overall gain of one.

IC704 guards the sensitive input lines to the buffer amplifier and reduces the capacitance to ground. It also provides switch-on drive for TR704, TR705 and TR706.

- 6.7 AC RMS CONVERTER (Sheet 5)
  The rms converter can be divided into two specific sections:
  - 1. The absoluter, which converts the alternating signal into one with a single polarity.
  - 2. The converter, that converts the varying single polarity input into a dc signal which represents the rms value of that input.

#### 6.7.1 The Absoluter

The absoluter consists of a fast virtual earth amplifier with a pair of diodes in the output that generate the positive and negative components of the output signal separately. The bandwidth of the rms converter depends primarily on the bandwidth of this circuit and, for this reason, it is constructed to be as fast as possible. To speed up the output transition, from positive to negative polarity, the two diodes are driven by a constant current stage.

The input current is generated by R750 and the feedback is through R750 or R753 depending on the polarity. The positive output voltage is added to the original input signal (but with twice the weighting) through R751. Thus, for an input of -S volts, the converter has an input current of:

$$\frac{-S}{10k} + \frac{2S}{10k} = \frac{S}{10k}$$

For an input of +S volts, the converter input current equals:

$$\frac{S}{10k} + \frac{OS}{10k} = \frac{S}{10k}$$

i.e. the input current is always positive.

The amplifier consists of two paths; a fast, low accuracy path and a slow, high accuracy path.

The fast path is through TR762 (a source follower), TR763 (an emitter follower), TR751 (common base) and TR764 which is the constant current output stage. The 100kHz frequency response is set by RV752. This component controls the phase shift of network C760, R759 and RV752 at 100kHz, and hence the gain.

The slow path is through integrator IC752. Change over from one path to the other occurs at 100kHz.

#### 6.7.2 The Converter

The basic amplifier is very similar to the absoluter amplifier, but with RV752 replaced with a fixed resistor (R767) and a variable resistor (RV753) added. This allows the gain bandwidth product to be adjusted and, in effect, allows the lMHz gain to be controlled.

A simplified circuit diagram of the converter is shown in Figure 6.2.

- i) Transistors A and B, in conjunction with IC753, produce a voltage at the emitters of B and C, which is equal to  $2\log_{\rm e} I_{\rm in}$
- ii) D develops a voltage at its emitter which is equal to log aV(I ), where av(I ) is the average value of out out Iout derived from the filter output.
- iii) The difference between (i) and (ii) is developed across the base emitter junction of C to produce I<sub>OUt</sub>:

$$\exp(2\log_e I_{in} - \log_e av(I_{out})) = I_{out}$$

which implies

$$\frac{I_{in}^2}{av(I_{out})} = I_{out}$$

(iv) This is filtered again, to give:

$$av[I_{in}^2 - av(I_{out})] = av[I_{out}]$$

which implies

$$avI_{n}^{2} = [av(I_{OUT})]^{2}$$

or

$$av(I_{out}) = \sqrt{avI_{in}^2}$$

In other words, the filter output (avI $_{out}$ ) is  $\sqrt{avI}_{in}$  which is simply the definition of the rms value of Iin.

To obtain good gain stability transistors A and D are a matched pair; similarly B and C. Any offset between these transistors appears as a gain error given by:

However, even the use of matched pairs can give a certain improvement only, particularly with respect to long term drift, so the circuit goes one stage further.

Transistor pair A and D are swapped over at a rate of 10Hz. similarly B and C. The effect can be seen mathematically, i.e. the output is given by

%exp(logeI + Voffset) + %exp (logeI - Voffset)

= % [lexp Voffset + lexp (-Voffset)]

For small values of  $V_{\mbox{\scriptsize offset}}$ , a Taylor expansion may be used, i.e.

exp 
$$V_{\text{offset}} \approx 1 + V_{\text{offset}} + \frac{V_{\text{offset}}}{2}$$

giving:

%[Iexp V<sub>offset</sub> + Iexp (-V<sub>offset</sub>)] = %I(2 + V<sub>offset</sub>)

$$= I(1 + \frac{Voffset}{2})$$

The unchopped error would have been:

$$I(1 + V_{offset} + \frac{V_{offset}}{2})$$

The components which achieve the switching are TR770 to TR779 inclusive. They are driven through resistors to minimise the transient disturbance by IC750, which switches between -15V and -1.3V. TR780 performs logic level shifting.

If the voltmeter is using an integration rate below 100ms on ac, a reading may be generated with the chopper in one of two states and no averaging effect will occur. Thus, as a result of  $V_{\mbox{offset}}$ , two possible outputs could occur, differing by more than one bit. For this reason, RV751, R791 and R790 are included to reduce the offset to a minimum.

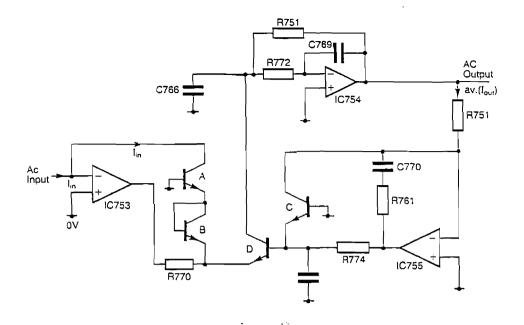


Figure 6.2 Converter

# 6.8 TEST POINTS

The following Test Points are provided to assist in printed circuit board fault-finding.

Table 6.2 Test Points

Test Point (TP)	Signal
101 102 103 104 105 106	HI LO DC Output Bootstrap OV Mytchett +15 Clamp
401 402 403 404 405	-15 Clamp  Bootstrap Chopper Output Demodulator Output Demodulator OV
702 705	AC Bootstrap Buffer Output
750 751 753 756 757	Rectifier Bias Log Bias Bias Log Drive RMS Output

### CHAPTER 7

# Component Parts Lists and Circuit Diagrams

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### Circuit Diagrams

PCB 1 PCB 3

PCB 4 and 8

PCB 5

PCB 6 and AC Linearity Modification (DCP)

PCB 14 and 8 (DCP)

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#### 7.1 INTRODUCTION

This chapter contains detailed Parts Lists and Circuit Diagrams for each of the printed circuit boards fitted in the instrument. When ordering spare parts, it is essential to quote the instrument serial number, located on the rear panel, as well as the full description shown in the appropriate parts lists.

#### 7.2 Component Parts List Abbreviations

#### 7.2.1 Circuit Reference

R - Resistor  $(\Omega)$ B - Battery

C - Capacitor (µF) RL - Relay

RNL - Non Linear Resistor  $(\Omega)$ CSR - Thyristor - Diode RV - Variable Resistor  $(\Omega)$ S - Switch

FS - Fuse IC - Integrated Circuit SK - Socket T ~ Transformer L - Inductor

LP - Lamp (including Neon) TP - Terminal Post (or Test Point)

TR - Transistor LK - Link

MSP - Mains Selector Panel X - Other components

PL - Plug

### 7.2.2 Component Types

#### Variable Resistors Fixed Resistors

CACP	Carbon Compositiion	CAFM	Carbon Front Panel Multiturn
CAFM	Carbon Film	CAFS	Carbon Front Panel Single Turn
CKCA	Cracked Carbon	CAPM	Carbon Preset Multiturn
MEFM	Metal Film	CAPS	Carbon Preset Single Turn
MEGL	Metal Glaze	CMFM	Cermet Front Panel Multiturn
MEOX	Metal Oxide	CMFS	Cermet Front Panel Single Turn
POWW	Power Wirewound	CMPM	Cermet Preset Multiturn
PRWW	Precision Wirewound	CMPS	Cermet Preset Single Turn
TEMP	Temperature Sensitive	CMPS	Cermet Preset Single Turn
TKFM	Thick Film	WWFM	Wirewound Front Panel Multiturn
TNFM	Thin Film	WWFS	Wirewound Front Panel Single Turn
VOLT	Voltage Sensitive	WWPM	Wirewound Preset Multiturn
	-	WWPS	Wirewoud Preset Single Turn

#### Capacitors

AIR	Air	MLAC	Metallised Lacquer
ALM	E Aluminimum Electolytic	PAPF	Paper Foil
ALM	S Aluminimum Solid	PAPM	Paper Metallised
CAR	B Polycarbonate	PTFE	PTFE
CER	M Ceramic	PYLN	Polyproylene Film
EST	F Polyester Foil	STYR	Polystyrene
EST	M Polyester Metallised	TAND	Tantalum Dry
MIC	A Mica	TANF	Tantalum Foil
GLA	S Glass	TANW	Tantalum Wet

PCB l Parts List

Cct Ref.		General De	scription		Solartron Part No.
R101 R102 R103 R104	CACP CACP CACP CACP	5Ω6 10k 10k 10k	1/2W 1/4W 1/4W 1/4W	10% 10% 10% 10%	172305600 172041000 172041000 172041000
C101 C102 C103 C104	CERM CERM CERM CERM	47n 47n 47n 100n	12V 12V 12V 40V	20% 20% 20% +80% -20%	241744700 241744700 241744700 208450140
C105	CERM	100n	40V	+80% -20%	208450140
C106	CERM	100n	40 <b>V</b>	+80% -20%	208450140
C107	CERM	330p	500V	20%	241323300
IC101 IC102 IC103 IC104	LS273 LS273 Resistor UDN6118	Pack, 150			510004380 510004380 160400587 510005710
IC105 IC106 IC107 IC108	UDN6118 LS74 UCN4810A UCN4810A				510005710 510002600 510005180 510005180
IC110 IC111 IC112 IC113	LS374 LS374 LS374 Resistor	Pack, 150			510004390 510004390 510004390 160400587
D101 to D122	LED				300750280
DS101	FG209M				300730460
PL101	Plug, 26	way			351326030
	Stick-on	Feet			420310260

PCB 3 Parts List

Cct Ref.		General D	escription		Solartron Part No.
R1	CACP	1k5	1/4W	10%	172031500
R2	CACP	1k5	1/4W	10%	172031500
R3	CACP	10k	1/4W	10%	172041000
R4	CACP	47k	1/4W	10%	172044700
R5	CACP	10k	1/4W	10%	172041000
R6	CACP	470	1/4W	10%	172024700
R7	CACP	150	1/4W	10%	172021500
R8	CACP	1k5	1/4W	10%	172031500
R9	CACP	1k	1/4W	10%	172031000
R10	CACP	3k3	1/4W	10%	172033300
R11	CACP	27k	1/4W	10%	172042700
R12	CACP	10k	1/4W	10%	172041000
R13	CACP	47k	1/4W	10%	172044700
R14	CACP	22k	1/4W	10%	172042200
R15	CACP	10k	1/4W	10%	172041000
R16	CACP	10k	1/4W	10%	172041000
R17	CACP	1k	1/4W	10%	172031000
R18	CACP	1k5	1/4W	10%	172031500
R19	CACP	15k	1/4W	10%	172041500
R51	CACP	100	1/4W	10%	172021000
R52	CACP	1k8	1/4W	10%	172031800
R53	MEFM	3k3	1/8W	0.5%	192733302
R54	CACP	100	1/4W	10%	172021000
R55	CACP	47k	1/4W	10%	172044700
R56	CACP	10k	1/4W	10%	172041000
R57	CACP	22	1/4W	10%	172012200
R58	CACP	22	1/4W	10%	172012200
R59	MEFM	470k	1/8W	0.5%	192754702
R60	CACP	1k8	1/4W	10%	172031800
R61	MEFM	3k3	1/8W	0.5%	192733302
R62	CACP	100	1/4W	10%	172021000
R63	CACP	47k	1/4W	10%	172044700
R64	CACP	10k	1/4W	10%	172041000
R65	MEFM	33k	1/8W	0.5%	192743302
R66	MEFM	12k	1/8W	0.5%	192741202
R67	MEFM	22k	1/8W	0.5%	192742202

PCB 3 Parts List (cont.1)

Cct Ref.		General Des	cription	Part No.	Solartron
R68 R69 R70 R71	MEFM MEFM POWW POWW	3k9 3k9 0Ω1 0Ω1	1/8W 1/8W	0.5% 0.5% 10% 10%	192733902 192733902 160200088 160200088
R72 R73 R74	MEFM CACP CACP	470k 1k5 1k5	1/8W 1/4W 1/4W	0.5% 10% 10%	192754702 172031500 172031500
C1 C2 C3 C4	CERM TAND VAR CERM	68p 4μ7 2 to 27p 22p	500V 10V 500V	20% 20% 20%	241316800 265464700 290030280 241312200
C5 C6 C10 C51 C52	CERM CERM TAND ALME ESTF	150p 100p 1µ 2200µ 4n7	500V 500V 35V 63V 100V	20% 20% 20% +50%-10%	241321500 241321000 266061000 208600264 227034700
C53 C54 C55 C56	ESTF TAND TAND ALME	10n 1μ 220μ 47μ	100V 35V 10V 40V	10% 20% 20% +50%-10%	227041000 266061000 265482200 273774700
C57 C58 C59 C60	ALME ALME ALME ALME	47µ 47µ 4700µ 22µ	40V 40V 50V 40V	+50%-10% +50%-10% +50%-10% +50%-10%	273774700 273774700 208600268 273772200
C61 C62 C64 C65	ESTM TAND ESTF ESTF	100n 10µ 4n7 10n	100V 25V 100V 100V	10% 10% 10%	225451000 208700108 227034700 227041000
C66 C67 C68 C69	TAND TAND ALME ESTM	1μ 220μ 220μ 100n	35V 10V 10V 100V	20% 20% +100%~10% 10%	266061000 265482200 273182200 225451000
C70 C71 to C78	ESTM CERM	100n 47n	100V 12V	10% +50%-25%	225451000 241744700
Bl	Battery				800400260

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PCB 3 Parts list (cont. 2)

Cct Ref.	General Description	Solartron Part No.
IC1	74LS04	510002690
IC2	74LS393	510004470
IC3	74LS08	510002910
IC4	74LS14	510003120
IC5	74LS196	510004710
IC6	74LS03	510004140
IC7	CD4040BE	510001820
IC8	74LS151	510002720
IC9	6402	510002820
IC10	6N136	300540150
IC11	6N136	300540150
IC12	Resistor pack 6.8k (15 off)	160400569
IC13	LS148	510005800
IC14	74LS157	510002240
IC15	74LS367	510003030
IC16	74LS74A	510002600
IC17	74F139	510005880
IC18	74LS74A	510002600
IC19	68A50	510003011
IC20	68A21	510002851
IC21	68A21	510002851
IC22	74L5240	510005310
IC23	74LS145	510004990
IC24	74LS30	510003560
IC25	LM301	510001270
IC26	MM58174N	510005480
IC27	LS32	510093140
IC28	LS107	510004550
IC29 IC51 IC52 IC55	LS164 TL494 THE TENENT TL494	510002890 510000690 510000500 510090690
IC56	LM311	510091280
TR1 TR2 TR3	BC214L 3N163 MPSA13	300554530
TR4	BC107	300553320
TR6	VN10KM	300555860
TR7	VN10KM	300555860

#<u>URMa</u>

# PCB 3 Parts List (cont.3)

Cct Ref.	General Description	Solartron Part No.
TR51 TR52 TR53 TR54	2N2907A BD131 2N2907A BD131	
TR55	U1897	300553800
TR56	U1897	300553800
D1	SD3	300522160
D2	SD3	300522160
D3	SD3	300522160
D51	WO4	300524700
D52	VSK340	300525850
D53	IN5339B	300526000
D54	WO4	300524700
D55	WO4	300524700
D56	C30	300521430
D57	VSK340	300525850
D58	IN5339B	300526000
D59	C5V6	300521450
D60	C12	300521480
D61	C12	300521480
PL1	Ribbon Plug, 40 way	352340110
PL2	Bergstik Plug, 15 way	352336070
PL3	Amp Header, 2 way	352302080
PL4	Ribbon Plug, 26 way	352326110
PL5	Ribbon Plug, 26 way	352326110
PL6	Ribbon Plug, 26 way	352326110
PL51	Amp Header, 8 way	352308060
PL52	Amp Header, 6 way	352306090
LS1	RM10 Inductor, 250µH	309511001
LS2	RM10 Inductor, 250µH	309511001
Nl	Mains Selector Mains Switch	550001480 375500020
Sl	8-pole DIL Switch	375000540
SK1	Socket, 40 way DIL	300585190
SK2	Socket, 40 way DIL	300585190
SK3	Socket, 40 way DIL	300585190
SK4	Socket, 24 way DIL	300584190
SK51	Socket, 16 way DIL	300584860

PCB 3 Parts List (cont.4)

Cct Ref.		Solartron Part No.		
FS1	Fuse	200mA	240V	360106280
FS2	Fuse	200mA	240V	360106280
Tl	Mains tr	ansformer		309617701
X1	Crystal	1.2288MHz		300810360
X2	Crystal	32.768kHz		300810640
TP1	Test Hoo	355400760		
TP2	Test Hoo	355400760		
TP3	Amp Disc	355900550		
TP4	Amp Disc	355900550		
TP5	Terminal		355500430	
TP6	Terminal		355500430	
TP51	Test Hoo		355400760	
TP52	Test Hoo		355400760	
TP53	Amp Disconnect Pin			355900550
TP54	Test Hook			355400760
TP55	Test Hook			355400760
TP56	Test Hook			355400760
TP57	Test Hoo	k		355400760
	PCB Hing PCB Edge	e (2) Support (2	2)	412011220 412011230

PCB 5 Parts List

Cct Ref.		General Des	scription		Solartron Part No.
R201 R202	MEFM MEFM	160k 100k	Matched P	recision	169616002
R203	MEFM	10k	1/8W	0.5%	192741001
R204	MEOX	lk	1/4W	5%	195631000
R205 R206	MEOX MEOX	lk 10 <b>0k</b>	1/4W 1/4W	5 <b>%</b> 5%	195631000 195651000
R207	MEOX	100k	1/4W	5%	195651000
R208	MEFM	10k	1/8 <b>W</b>	0.5%	192741001
R209 R210	MEFM MEOX	10k 10k	1/8W	0.5%	192741001
R210	MEOX	560	1/4W 1/4W	5 <b>%</b> 5%	195641000 195625600
R212	MEOX	10k	1/4W	5%	195641000
R213	MEOX	560	1/4W	5%_	195625600
R214 R215	MEFM MEFM	680 680	1/8W 1/8W	0.5% 0.5%	192726802 192726802
R217	MEOX	22k	1/4W	5%	195642200
R218	MEOX	22k	1/4W	5%	195642200
R219	MEOX	2k2	1/4W	5%	195632200
R220 R221	MEOX MEFM	2k2 39 <b>k</b>	1/4W 1/8W	5% 0.5%	195632200 192743902
-					
R222 R224	MEFM MEOX	100k 68	1/8W 1/4W	0.5% 5%	192751001 195616800
R301	MEFM	47k	1/8W	2%	160400571
R302	MEFM	470	1/8W	2%	192124700
R303	MEFM	4k7	1/8W	0.5%	192734704
R304 R305a	(To Mefm	be fitted of	only if sup Matched P	plied with	
R305b	MEFM	10k	Pair	recision	169616102
R306a	MEFM	6k			
R306b	MEFM	12k7	Matched P	recision	169616201
R306c R306d	mefm Mefm	600 300	Set		
R308 R309	CACP CACP	100 100	1/8W · 1/8W	10% 10%	172021000 172021000
R310	CACP	lk	1/8W	10%	172031000
R311	CACP	lk	1/8W	10%	172031000
R351	MEFM	33k	1.8W	0.5%	192743302
R352 R353	MEOX MEOX	6k8 10k	1/4W 1/4W	5% 5%	195636800 195641000
R354	MEFM	82k	1/8W	0.5%	192748202

R222 is 270k in early meters (DCP)

R304 is factory selected nominal value 3k (DCP)

PCB 5 Parts List (cont.1)

Cct Ref.		Genera	l Description		Solartron Part No.
R355 R501 R502 R503	MEFM Network Network MEFM	100 680 47k 470	1/8W	0.5%	192721002 160400570 160400571 192124700
R504	CACP	10k	1/8W	10%	172041000
R505	CACP	3k3	1/8W	10%	172033300
R506	MEFM	470	1/8W	2%	192124700
R507	MEFM	470	1/8W	2%	192124700
R509	CACP	1k	1/8W	10%	172031000
R601	MEOX	2k2	1/4W	5%	195632200
R602	MEOX	2k2	1/4W	5%	195632200
R603	MEFM	100k	1/8W	0.5%	192751001
R604 R605 R606 R607a R607b	MEFM MEOX Network	100k 100k 56k 47k	Precision 1/8W 1/4W 1.8W	0.5% 5% 2%	169616402 192751001 195645600 160400571
R608 R609 R611 R612	MEOX MEFM MEFM MEFM	1M 30k 600k 6k	1/2W Matched Precisi	l% on Set	195461000 169616303
R614	POWW	12k	2W	5%	193041200
R615	MEFM	470	1/8W	2%	192124700
R616	MEOX	10k	1/4W	5%	195641000
R617	MEOX	10k	1/4W	5%	195641000
R801	CACP	150	1/4W	10%	172021500
R802	CACP	3k3	1/4W	10%	172033300
R803	CACP	3k3	1/4W	10%	172033300
R804	CACP	22k	1/4W	10%	172042200
R805	CACP	47k	1/4W	10%	172044700
R806	CACP	1M	1/4W	10%	172061000
R807	CACP	100k	1/4W	10%	172051000
R808	CACP	100k	1/4W	10%	172051000
R809	CACP	220k	1/4W	10%	172052200
R810	CACP	100k	1/4W	10%	172051000
R811	CACP	47k	1/4W	10%	172044700
R812	CACP	470	1/4W	10%	172024700
R813	CACP	10k	1/4W	10%	172041000
R814	CACP	1k	1/4W	10%	172031000
R815	CACP	100	1/4W	10%	172021000
R816	CACP	330	1/4W	10%	172023300

PCB 5 Parts List (cont.2)

Cct Ref.		General Des	cription		Solartron Part No.
R817 R818 R819 R820	CACP CACP CACP CACP	27k 47k 47k 3k3	1/4W 1/4W 1/4W 1/4W	10% 10% 10% 10%	172042700 172044700 172044700 172033300
R821 R822 R823 R824	CACP CACP CACP CACP	10k 680 10k 2k7	1/4W 1/4W 1/4W 1/4W	10% 10% 10% 10%	172041000 172026800 172041000 172032700
R825 R826 R827	CACP CACP CACP	6k8 6k8 1k	1/4W 1/4W 1/4W	10% 10% 10%	172036800 172036800 172031000
C201 C202 C203 C204	PROP ESTM ESTM CERM	100n 470n 68n 150p	200V 100V 100V 500V	1% 10% 10% 20%	208100180 225454700 225446800 241321500
C205 C208	estm Cerm	10n 10n	100V 500V	10% +80% -20%	225441000 241941000
C209	CERM	10n	500V	+80% -20%	241941000
C210	CERM	2n2	500V	+40% -20%	241332200
C211.	CERM	2n2	500V	+40% -20%	241332200
C212 C213 C214	ESTM TAND ESTM	470n 47µ 100n	100V 20V 100V	10% 10% 10%	225444700 265774700 225451000
C215 C216	estm Cerm	100n 47n	100V 25V	10% +50% -25%	225451000 241944700
C217	CERM	47n	25 <b>V</b>	+50% -25%	241944700
C218	CERM	47n	25V	+50% -25%	241944700
C219	CERM	47n	25V	+50% -25%	241944700
C220	CERM	470p	500V	20%	241324700
C221	CERM	470p	500V	20%	241324700
C223	TAND	22μ	35V	10%	265972200

PCB 5 Parts List (cont.3)

Cct Ref.		General D	escription		Solartron Part No.
C301	CERM	47n	25V	+50% -25%	241944700
C302	CERM	47n	25V	+50% -25%	241944700
C303 C304	CERM CERM	10p 10p	500V 500V	20% 20% 20%	241311000 241311000
C305 C306 C351	CERM CERM CERM	10p 22p 10n 10n	500V 500V 25V	20% 20% +50% -25% +50%	241311000 241322000 241941000
C352	CERM	1011	250	+50% -25%	241941000
C501 C502 C503 C601	ESTM ESTM ESTM ESTM	10n 100n 100n 100n	100V 100V 100V 100V	10% 10% 10% 10%	225441000 225451000 225451000 225451000
C602 C603 C604 C605	ESTM ESTM ESTM ESTM	100n 100n 100n 10n	100V 100V 100V 100V	10% 10% 10% 10%	225451000 225451000 225451000 225441000
C606 C607 C608 C609	ESTM ESTM ALME	10n 100p 33n 100	100V 100V 400V 100V	10% 20% 10% +100% -10%	225441000 208900004 226043300 273981000
C610	ALME	47μ	100V	+100% -10%	273974700
C611 C612	CERM CERM	10n 10n	250V 25V	+50% -25%	208450036 241941000
C613	CERM	10n	250V		208450036
C614 C615 C616	estm estm cerm	100n 100n 47n	100V 100V 25V	10% 10% +50% -25%	225451000 225451000 241944700
C617	CERM	47n	25V	+50% -25%	241944700
C801 C802 C803	CERM CERM CERM	22p 22p 22n	500V 500V 25V	20% 20% +50% -20%	241312200 241312200 241842200
C804	ALME	47μ	40V	+50% -10%	273774700

	Parts Li	st (cont.4)			
Cct Ref.		General De	escription		Solartron Part No.
C805	TAND	4µ7	10V	20%	265464700
C806	TAND	100ս	10V	20%	265481000
C807	VAR	6-30p	160V	10%	290020450
C808	CERM	10p	250V	20%	208450000
0000	Oblui	101	2501	203	200430000
C809	CERM	3n3	500V	+40% -20%	241333300
C810	CERM	330p	500 <b>V</b>	10%	208450060
C811	CERM	47n	12 <b>V</b>	+50%	241744700
				-25%	212/11/00
C812	TAND	47µ	6 <b>V</b>	20%	265274700
		- · p	•	200	203214100
C813	CERM	ln	500V	+40%	241331000
				-20%	
C814	TAND	lμ	35V	20%	266061000
C815	ESTM	100n	100V	10%	225451000
_C816	CERM	47n	12V	+50%	241744700
				-25%	
0017	CEDM	47-	100	. 500	241744700
C817	CERM	47n	12V	+50%	241744700
-010		4.5		-25%	
C818	CERM	47n	12V	+50%	241744700
				-25%	
a010	20014	47	104-		
C819	CERM	47n	12V	+50%	241744700
		45	1011	-25%	
C820	CERM	47n	12 <b>V</b>	+50%	241744700
		•		−25%	
a021	GDDW.	00	5000	. 400	0.11.000000
C821	CERM	3n3	50 <b>0</b> V	+40%	241333300
<b>4022</b>	(III) A III)	22	1 617	-20%	000700106
C822	TAND	22µ	16V		208700106
C823	CERM	47n	12V	+50%	241744700
		_		-25%	
C824	CERM	47n	12V	+50%	241744700
				-25%	
2005		4.5			<b></b>
C825	CERM	47n	12V	+50%	241744700
-0.0.5				-25%	
C826	CERM	47n	12V	+50%	241744700
-001			4.0	-25%	
C901	ALME	220 µ	40V		208600262
C902	ALME	220 μ	40V		208600262
<b>~</b> 0.00		1000			
C903	ALME	1000µ	40V		208600263
C904	ALME	1000µ	40V		208600263
C905	ALME	220ր	40V		208600262
C906	ALME	220ր	40V		208600262
C907	TAND	Lμ	35V	20%	266061000
C908	TAND	lμ	35V	20%	266061000
C909	TAND	lμ	35V	20%	266061000
C910	TAND	$1\mu$	35V	20%	266061000
0142a/Ju	IC.		7 12		

2890g/0142g/JWS

Cct Ref.		General	Description	n	Solartron Part No.
C912	TAND	220	10V	20%	265482200
IC201 IC202 IC203 IC204	ICL7650 LM301 LM311 LM311	BCPD			510091810 510091270 510091280 510091280
IC205 IC301 IC302 IC303	74S175 AD7533JI ILQ74 ILQ74	N			510003460 510090670 300540250 300540250
IC304 IC305 IC306 IC307	741CH 0P07EZ 0P07EZ DG301		,		510091310 510091420 510091420 510091110
IC351 IC352 IC501 IC502	MC1458 CA3046 ILQ74 ICL7650	BCPD			510091300 300554090 300540250 510091810
IC503 IC601 IC602 IC603	78L12 ICL7650 ICL7650 LH0052				510090450 510091810 510091810 510090260
IC604 IC605 IC606 IC607	ICL7650 ILQ74 TIL111 78L15	BCPD			510091810 300540250 300540140 510090420
IC608 IC801 IC802 IC803 * On la	79L15 63A03MP LS373 2564* ter mode		o. 2764 is	used.	510090430 510006170 510004870 510005610
IC804 IC805 IC806 IC807	ER3400 F138 LS74A LS191				510005600 510005870 510002600 510004190
IC808 IC809 IC810 IC811	LS374 LS374 LS191 LS191				510004390 510004390 510004190 510004190
IC812 IC813 IC814 IC815	LS191 LS163 LS393 LS393				510004190 510004170 510004470 510004470

PCB 5 Parts List (cont.6)

Cct Ref.	General Description	Solartron Part No.
IC816	LS273	510004380
IC817	LS273	510004380
IC818	LS273	510004380
IC819	LS393	510004470
IC820	LS163	510004170
IC821	LS00	510002000
IC822	LS02	510002230
IC823	LS04	510002690
IC824	CD4046	510005690
IC825	Resistor Pack, 6.8k	160400569
IC826	TC5516P	510005470
IC827	LS161AN	510004160
IC829	ULN2003A	510004980
IC830	LS273	510004380
IC831	F138	510005870
IC833	LS153	510002740
IC834	LS132	510002980
IC835	LS74	510002600
IC901	7815CT	510090320
IC902	7915CT	510090330
IC903	7812CT	510090520
IC904	7912CT	510090530
TR201	VN67AK	300555940
TR202	VN67AK	300555940
TR203	3N163	300554530
TR204	3N163	300554530
TR205	BCY70	300553590
TR206	BCY70	300553590
TR207	VN10	300555860
TR208	VN10	300555860
TR301	BC107	300553320
TR302	BCY70	300553590
TR504	U1897	300553800
TR505	VN67AK	300555940
TR506	VN67AK	300555940
TR508	VN67AK	300555940
TR509	VN67AK	300555940
TR510	U235	300553810
TR512	U1897	300553800
TR513	U1897	300553800

Cct Ref.	General Description	Solartron Part No.
TR516	U1899 VN67AK VN67AK U1899	300554320 300555940 300555940 300554320
TR519	U1899	300554320
TR601	U1899	300554320
TR602	U1899	300554320
TR603	3N163	300554530
TR604	WM222	300555940
TR605	3N171	300555270
TR606	2N4118A	300555880
TR607	2N4118A	300555880
TR608 TR609 TR610 TR801		300555880 300555380 300554530 300553590
TR802	BC107	300553320
TR803	2N2484	300552860
TR804	BC107	300553320
TR805	2N2369	300552390
TR806	BCY70	300553590
TR807	2N2369	300552390
D204 D205 D301	Zener, 7.5V Zener, 7.5V Reference Zener*	300521460 300521460 70818008A (for 7071 only) 70818007A
failure	al selection during test. Ava e only. Package may include a ected, on test, to match diode	resistor (R304), whose value
D302	Zener, 10V	300522760
D351	AD590K	510090760
D352	SD3	300522160
D353	SD3	300522160
D501	DPAD10	300525870
D502 D503 D504 D505	DPAD10 Zener, 6.8V Zener, 15V Zener, 15V	300525870 300522540 300521390 300521390
D507	Zener, 5.6V	300521450
D601	WR057	300525770

D602

WR057

300525770

PCB 5 Parts List (cont.8)

Cct Ref.	General Description	Solartron Part No.
D603	DPAD10	300525870
D604	Zener, 8.2V	300521330
D605	DPAD10	300525870
D606	SD3	300522160
D607	SD3	300522160
D608	LED	300750080
D609	DPAD10	300525870
D610	IN4007	300524990
D611	IN4004	300522070
D612	IN4004	300522070
D613	Zener, 10V	300522760
D614	Zener, 10V	300522760
D615	Zener, 3.9V	300521420
D616	WR057	300525770
D617	WR057	300525770
D801	SD3	300522160
D802	SD3	300522160
D803	SD3	300522160
D804	C8V2	300521330
D805	SD3	300522160
D806	SD3	300522160
D807	C3V6	300523890
D808	MV2110	300525320
D809	MV2110	300525320
D810	SD3	300522160
D901	Bridge W04	300524700
D902	IN4004	300522070
D903	IN4004	300522070
D904	IN4004	300522070
D905	IN4004	300522070
RL1	Coto Relay	300652230
RL501	Coto Relay	300652230
L801	Inductor, 33µH	305020440
L802	Inductor, 3.9µH	305020750
PL501	Plug, 34 Way	352334050
PL502	Plug, 10 Way	352310070
PL504	Plug, 4 Way	352304080
SK801	Socket, 40 Way DIL	300584970
SK802	Socket, 28 Way DIL	300585120
SK804	Socket, 22 Way DIL	300584980
SK806	Socket, 24 Way DIL	300584740

# PCB 5 Parts List (cont.9)

Cct Ref.	General Description	Solartron Part No.
SK901	Socket, 16 Pin DIL	300584860
sl	Switch, 6-pole DIL	375000570
X801	Crystal, 4.9152MHz	300810590
TP201 to TP205	Test Hook	355400760
TP301 to TP305	Test Hook	355400760
TP501 to TP505	Test Hook	355400760
TP601 to TP609	Test Hook	355400760
TPl to TP6	Test Hook	355400760
TP901 to TP906	Test Hook	355400760
	Transistor Pads Diode Pad Heat Sink	300584090 300584220 300584940

PCB 6 Parts List

Cct Ref.		General	Description		Solartron Part No.
Rl to	MEFM	3M3 <sup>-</sup>	Was also I Bu		150415000
R3 R4	MEFM MEFM	100k	Matched Pr	ec. Set	169615802
R5	MEFM	18k		0.1%	160300503
R6 R7	MEFM CACP	18k 56	1/2W	0.1% 10%	160300503 172315600
R101	MEFM	10k	1/8W	0.5%	192741002
R102	MEFM	24k	1/8W	0.5%	192742402
R103 R104	MEFM MEFM	10k 4k7	1/8W	0.5%	192741002 160300501
R105	MEFM	47k	1.8W	2%	160400571
R107	MEOX	47k	1/4W	5%	195644700
R109	MEFM	470	1/8W	2%	192124700
R110	CACP	lk	1/8W	10%	172031000
Rlll	MEFM	9k	Watehad De	an Gab	160615000
R112 R113	MEFM MEFM	1k1 9k	Matched Pr	ec. Set	169615902
R113	MEFM	lkll			
11421	115111	21122			
R401	MEFM	33k	1/8W	0.5%	192743302
R402	MEFM	33k	1/8 <b>W</b>	0.5%	192743302
R403	CACP	lk	1/4W	10%	172031000
R404	MEFM	470k	1/8W	0.5%	192754702
R405	MEFM	15k	1/8W	0.5%	192741502
R406	MEFM	470k	1/8W	0.5%	192754702
R407	PRWW	15k			160300502
R408	PRWW	15k			160300502
R409	MEFM	270k	1/8 <b>W</b>	0.5%	192752701
R410	MEFM	1M	1/4W	1%	198361002
R411	MEFM	1M	1/4W	1%	198361002
R412	MEFM	100k	1/8W	0.5%	192751002
R413	MEFM	100k	1/8W	0.5%	192751002
R414	MEFM	100k	1/8W	0.5%	192751002
R415	MEFM	lM	1/4W	1%	198361002
R416	MEFM	lM	1/4W	1%	198361002
R421	MEFM	100k	1/8W	0.5%	192751002
R422	MEFM	680	1/8W	0.5%	192726802
R423	MEFM	15k	1/8W	0.5%	192741502
R424	MEFM	100k	1/8W	0.5%	192751002

PCB 6 Parts List (cont.1)

Cct Ref.		General Des	cription		Solartron Part No.
R425	Mefm	lm	1/4W	1%	198361002
R426	Mefm	lm	1/4W	1%	198361002
R427	Mefm	lm	1/4W	1%	198361002
R428	Mefm	lok	1/8W	0.5%	192741002
R701	mefm	47k	1/8W	0.5%	192744102
R702	Megl	47k	3W	2%	175244700
R703 R707 R708	Mefm Mefm Mefm	990k 9k 1k	Matched Se	t	169616601
R705a-g	MEFM	10k	1.8W	2%	192141000
R706	CACP	1k	1/2W	10%	172031000
R709	MEFM	470k	1/8W	0.5%	192754702
R710	MEFM	5k1	1/8W	0.5%	192735102
R711	CACP	lm	1/2W	10%	172361000
R712	MEOX	3k3	1/4W	5%	195633300
R713	MEOX	3k3	1/4W	5%	195633300
R714	MEOX	47k	1/4W	5%	195644700
R715	MEOX	47k	1/4W	5%	195644700
R716	CACP	2k2	1/4W	10%	172032200
R718	CACP	100	1/8W	10%	172021000
R720	CACP	560	1/4W	10%	172025600
R721	CACP	4k7	1/4W	10%	172034700
R722	CACP	1k	1/2W	10%	172331000
R723	CACP	22 <u>M</u>	1/2W	10%	172372200
R724	MEFM	965k	1/4W	0.5%	160400530
R725	MEFM	405k/500	Matched Pa	ir	160400604
R729	MEFM	33k	1/8W	0.5%	192743302
R750	Caddock	Network 5k/	5k	0.1W/R	160400605
R751A R751B R753 R754 R755		Network 10k Network 50k 5kl 5kl 6k8		0.1W/R 0.5% 0.5% 5%	160400606 160400606 192735102 192735102 195636800
R756	MEOX	2k2	1/4W	5%	195632200
R757	CACP	220	1/8W	10%	172022200
R758	MEFM	47	1/8W	0.5%	192714702
R759	MEOX	220	1/4W	5%	195622200
R760	MEOX	1k	1/4W	5%	195631000
R761	MEOX	33k	1/4W	5%	195643300
R762	CACP	1k	1/8W	10%	172031000
R763	MEOX	6k8	1/4W	5%	195636800

	Parts Lis	t (cont.2)			
Cct Ref.		General De	escription		Solartron Part No.
R764	MEOX	lk	1/4W	5%	195631000
R765	CACP	220	1/8W	10%	172022200
R766	MEFM	47	1/8 <b>W</b>	0.5%	192714702
R767	MEOX	560	1/4W	5%	195625600
R768	MEOX	1k	1/4W	5%	195631000
R770	MEFM	1k	1/8W	0.5%	192731002
R771	MEOX	100k	1/4W	5%	195651000
R772	MEFM	39k	1/8W	0.5%	192743902
R774	MEFM	lk	1/8W	0.5%	192731002
R775 R776	MEOX	10k 10k	1/4W	5% 5%	195641000
R//0	MEOX	IUK	1/4W	23	195641000
R778	MEOX	10k	1/4W	5%	195641000
R779	MEOX	10k	1/4W	5%	195641000
R780		10k	1.8W	2%	192141000
R781	MEOX	10k	1/4W	5%	195641000
R782	MEOX	10k	1/4W	5%	195641000
R784	CACP	lk	1/8 <b>W</b>	10%	172031000
R785	CACP	5Ω6	1/2W	10%	172305600
R786	CACP	5Ω6	1/2W	10%	172305600
R787	CACP	220	1/8W	10%	172022200
R788	CACP	220	1/8W	10%	172022200
R790	Mefm	10	1/8W	0.5%	192711002
R791	MEFM	330k	1/8W	0.5%	192753302
RV701	CMPM	5 <b>k</b>	1/2 <b>W</b>	10%	130935000
RV751	CMPM	100k	1/2W	10%	130951000
RV752	CMPM	500	1/2W	10%	130925000
RV753	CMPM	100	1/2W	10%	130921000
Cl	estf	22n	400V	10%	222342200
ClOl	CERM	3n3	500V	20%	241333300
C102	CERM	3n3	50 <b>0V</b>	20%	241333300
C103	ESTF	ln .	400V	10%	222331000
C401	CERM	3n3	500V	20%	241333300
C404	ESTM	22n	10 <b>0</b> V	10%	225442200
C405	ESTM	100n	100V	10%	225451000
C406	ESTM	100n	V001	10%	225451000
C407	TAND	4µ7	35V	20%	266064700
C408	ESTM	220n	100V	10%	225452200
C409	ESTM	220n	100V	10%	225452200
C410	ESTM	2μ2	100V	10%	225462200
C411	ESTM	2µ2	100V	10%	225462200
C412	ESTM	1	100V	10%	225461000
C413 C414	CERM	10n	25V	+50%-25%	
0414	CERM	47n	25V	+50%-25%	241944700

PCB 6 Parts List (cont.3)

Cct Ref.		General De	scription		Solartron Part No.
C415	CERM	10n	25V	+50%-25%	241941000
C416	CERM	47n	25V	+50%-25%	241944700
C701	ESTM	220n	1000V	20%	226752200
C702	ESTM	220n	100V	10%	225452200
C703	TAND	lu5	20V	20%	265861500
C704	CERM	22p	500V	20%	241312200
C705	ESTF	10n	100V	10%	225441000
C708	CERM	10n	25V	+50%-20%	241941000
C709 C712 C714 C716	ESTF CERM TAND TAND	10n 2p2 10 4µ7	1000V 25V 35V	10% 20% 20%	222841000 208450094 208700108 208700109
C717	TAND	4µ7	35V	20%	208700109
C718	CERM	47n	25V	+50%-20%	241944700
C719	CERM	47n	25V	+50%-20%	241944700
C720	CERM	10n	25V	+50%-20%	241941000
C721	CERM	10n	25V	+50%-20%	241941000
C751	ESTF	3n3	400V	10%	222333300
C755	CERM	47n	25V	+50%-20%	241944700
C756	CERM	47n	25V	+50%-20%	241944700
C757	TAND	lμ	35V	20%	266061000
C758	STYR	150p	125V	10%	210221500
C759	CERM	10n	25V	+50%-20%	241941000
C760	ESTF	3n3	400V	10%	222333300
C761	TAND	l	35V	20%	266061000
C762	CERM	47n	25V	+50%-20%	241944700
C763	CERM	47n	25V	+50%-20%	241944700
C764	STYR	150p	125V	10%	210221500
C765	CERM	10p	500V.	20%	241311000
C766	ESTM	220n	100V	10%	225452200
C767	ESTM	4µ7	63V	10%	225164700
C768	ESTM	4µ7	63V	10%	225164700
C769	ESTM	220n	100V	10%	225452200
C770	CERM	ln	500V	+40%-20%	241331000
C771	TAND	2µ2	20V	20%	265862200
C775	CERM	10p	500V	20%	241311000
IC101 IC102 IC103 IC104	TIL111 LM343D LM343D ILQ74				300540140 510091140 510091140 300540250

Cct Ref.	General Description	Solartron Part No.
IC401	CA3183AE	300555390
IC402	LM343D	510091140
IC403	LM343D	510091140
IC404	OPO5CP	510091130
IC405 IC406 IC701	LH0052 4093 9D8-CC	510090260 510001780
IC702	7406	510000760
IC703	7406	510000760
IC704	LM310	510090040
IC705	OP16FJ	510091370
IC706	LM339	510090490
IC750	4093	510001780
IC752	OP-07EZ	510091420
IC753	OP-07EZ	510091420
IC754	OP-07EZ	510091420
IC755	OP-07EZ	510091420
TR101	WN1001	300555770
TR102	WN1001	300555770
TR103	WN1001	300555770
TR104	P1087	300555550
TR105	UI897	300553800
TR106	UI897	300553800
TR107	UI897	300553800
TR401	WD401	300555370
TR404	MATO1GH	300555930
TR405	2N4303	300553160
TR406	PN4117A	300555950
TR407	PN4117A	300555950
TR408	PN4117A	300555950
TR409	Zener, 16V	300521320
TR410	Zener, 16V	300521320
TR412	2N5905	300554230
TR702	BCY70	300553590
TR703	BFY90	300553890
TR704	U1899	300554320
TR705	U1899	300554320
TR706	U1899	300554320
TR751	BCY70	300553590
TR752	BCY70	300553590
TR755	BCY70	300553590
TR756	BCY70	300553590

PCB 6 Parts List (cont.5)

Cct Ref.	General Description	Solartron Part No.
TR758	MATOIGH	300555930
TR759	MATOIGH	300555930
TR760	U1897	300553800
TR761	U1897	300553800
TR762	U1899	300554320
TR763	2N2369	300552390
TR764	BFY90	300553890
TR765	U1899	300554320
TR766	2N2369	300552390
TR767	BFY90	300553890
TR770	U1897	300553800
TR771	U1897	300553800
TR772	U1897	300553800
TR773	U1897	300553800
TR774	U1897	300553800
TR775	U1897	300553800
TR776	U1897	300553800
TR777	U1897	300553800
TR778	U1897	300553800
TR779	U1897	300553800
TR780	U1899	300554320
D101	DPAD1	300525930
D102	Zener, 16V	300521320
D103	Zener, 16V	300521320
D104	J511	300526040
D105	Zener, 5V1	300521310
D106	J507	300525820
D107	SD3	300522160
D108	SD3	300522160
D109	WRO57	300525770
D110	WRO57	300525770
D111 -"	Zener, 12V	300521480
D112	SD3	300522160
D113	SD3	300522160
D114	Zener, 12V	300521480
D401	WRO57	300525770
D402	J507	300525820
D403	IN821	300522460
D404	Zener, 3V3	300521860
D405	Zener, 5V1	300521310
D406	J507	300525820

PCB 6 Parts List (cont.6)

Cct Ref.	General Description	Solartron Part No.
D407 D408 D409 D410	wr057	300525820 300525770 300521320 300521320
D711	Zener, 12V	300521480
D712	IN3595	300523590
D713	IN3595	300523590
D714	Zener, 12V	300521480
D715	SD3	300522160
D716	Zener, 8V2	300521330
D717	J511	300526040
D750	HP5082-6221	300525380
D751 D752 D753 D754	Zener, 5V6	300525380 300521450 300523590 300523590
D755	SD3	300522160
D756	SD3·	300522160
RL2	Coto Relay 1240-0145	300652250
RL3	Coto Relay 1240-0145	300652250
RL4	Coto Relay 3400-0011	300652270
RL5	Coto Relay 3400-0051	300652290
RL6	Coto Relay 1240-0144	300652260
RL7	Coto Relay 1285-0051	300652310
RL701	Coto Relay 7002-5082	300652300
R1702	Coto Relay 4000-0119	300652320
RL703	Coto Relay 4000-0119	300652320
RL704	Coto Relay CR-4010-5-1011	300652200
RL705	Coto Relay CR-4002-5-1011	300652210
RL706	Coto Relay CR-4002-5-1011	300652210
RL707	Gentech Relay 831C-1	300652180
sl	Front/Rear Switch	377000410
SGl	Spark Gap	300011470
PL603	Amp Mod, 6 Way	352306090
TL1	Turret Lug	355500430
TL2	Turret Lug	355500430

PCB 6 Parts List (cont.7)

Cct Ref.	General Description	Solartron Part No.
TP101 to TP107	Test Hook	355400760
TP401 to TP405	Test Hook	355400760
TP702 TP705 TP750	Test Hook Test Hook	355400760 355400760
to TP753	Test Hook	355400760
TP756 TP757	Test Hook Test Hook	355400760 355400760
	Ceramic Beads Ceramic Beads Heatsink	470120100 470120040 300584200

# PCB 8 Parts List

Cct Ref.	General Description	Solartron Part No.
IC801	Resistor Pack, 22k	160400589
SK801	Socket, 16 Way DIL	300584860
S <b>W</b> 801	Switch, 8 Way DIL	375000600

PCB 4 & PCB 14 Parts List

Cct Ref.		General De	scription		Solartron Part No.
R401 R402 R403 R404	CACP CACP CACP CACP	100k 100k 470 820	1/4W 1/4W 1/4W 1/4W	10% 10% 10% 10%	172051000 172051000 172024700 172028200
R405 R406	CACP CACP	150 3k3 .	1/4W 1/4W	10% 10%	172021500 172033300
C401 C402 C403 C404	CERM CERM CERM CERM	22p 22p 47n 47n	500V 500V 12V 12V	20% 20% 20% 20%	241312200 241312200 241744700 241744700
C405 C406 C407 C408	CERM CERM CERM CERM	47n 47n 47n 47n	12V 12V 12V 12V	20% 20% 20% 20%	241744700 241744700 241744700 241744700
C409 C410 C411 C412	TAND TAND CERM CERM	4μ7 33μ 47n 47n	10V 10V 12V 12V	20% 20% 20% 20%	265464700 265473300 241744700 241744700
IC401 IC402 IC403 IC404	MC68B09P MC68A44 74LS02 Resistor				510005121 510005031 510002230 192112200
IC405 IC406 IC407 IC408	Resistor TC5516P TC5516P TC5516P	Pack, 6.8	k		160400569 510005470 510005470 510005470
IC409 IC410 IC411 IC412	TC5516P TC5516P TC5516P TMS2564*				510005470 510005470 510005470 510005610
IC413 IC414 IC415 IC416	TMS2564* TMS2564* TMS2564* 74LS138			·	510005610 510005610 510005610 510003530
IC417 IC418 IC419 IC420	74LS138 74LS138 74LS157 8291				510003530 510003530 510002240 510005590

<sup>\*</sup> On later models Part No. 2764 is used. 510006280

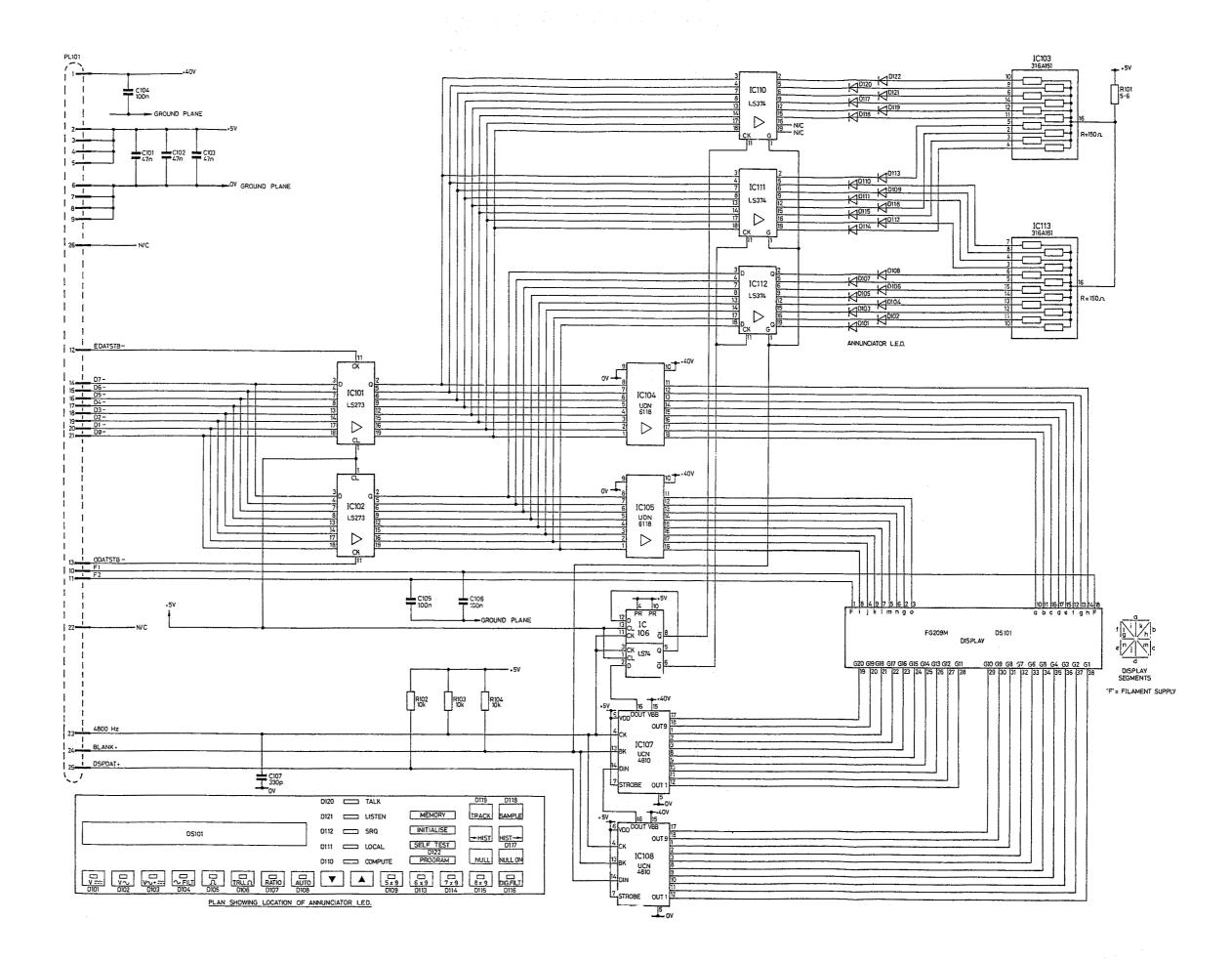
PCB 4 & PCB 14 Parts List (cont. 1)

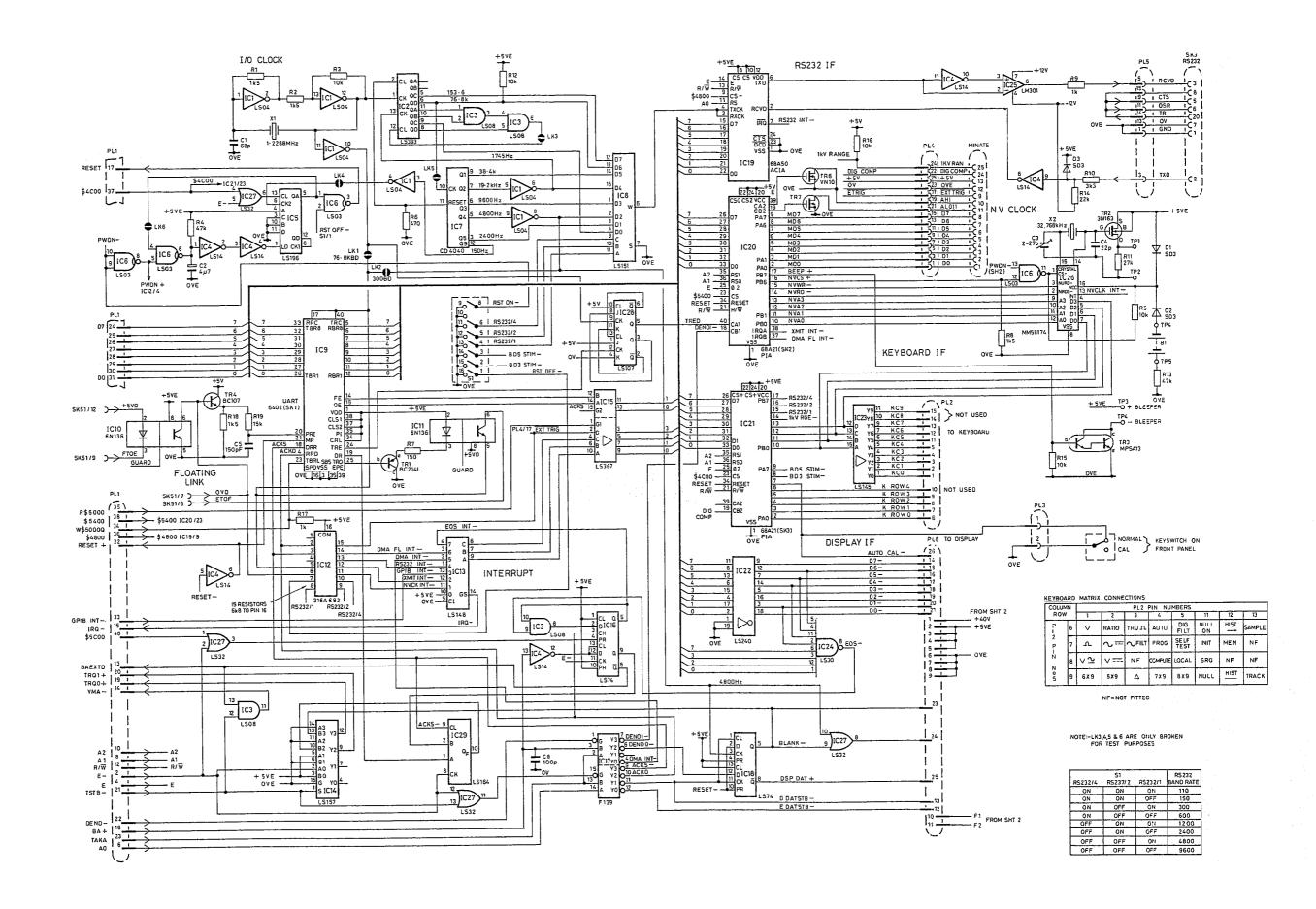
Cct Ref.	General Description	Solartron Part No.
IC421 IC422 IC424 IC430	MC3447 MC3447 74LS244 TMS2564*	510005700 510005700 510004500 510005610
TR401 TR402 TR403	BCY70 BC107 2N2369	300553590 300553320 300552390
D401 D403 D404	SD3 SD3 Zener, 3.3V	300522160 300522160 300521860
SK401 SK402 SK403 SK404	Socket, 28 Way DIL	300585190 300585160 300585160 300585160
SK405 SK406 SK407 SK408	Socket, 28 Way DIL Socket, 28 Way DIL Socket, 28 Way DIL Socket, 24 Way DIL	300585160 300585160 300585160 300584910
SK409 SK410 SK411 SK412	Socket, 24 Way DIL Socket, 24 Way DIL Socket, 24 Way DIL Socket, 24 Way DIL	300584910 300584910 300584910 300584740
SK413 SK414a SK414b SK415 SK424 SK430	Socket, 40 Way DIL Socket, 16 Way DIL Socket, 40 Way DIL Socket, 20 Way DIL	300584900 300585190 300584860 300585190 300585220 300585160
B401	Battery, 3.6V, 90mA/hr	800400210
PL401 -	Plug and Ribbon Cable	70810204
X401	Crystal, 6MHz	300810560
TP1 to TP6 TP7	Test Hook Amp. Disc. Pin	355400760 355900550
TP8 TP9	Test Hook Test Hook	355400760 355400760
* On la	ter models Part No. 2764 is used.	510006280

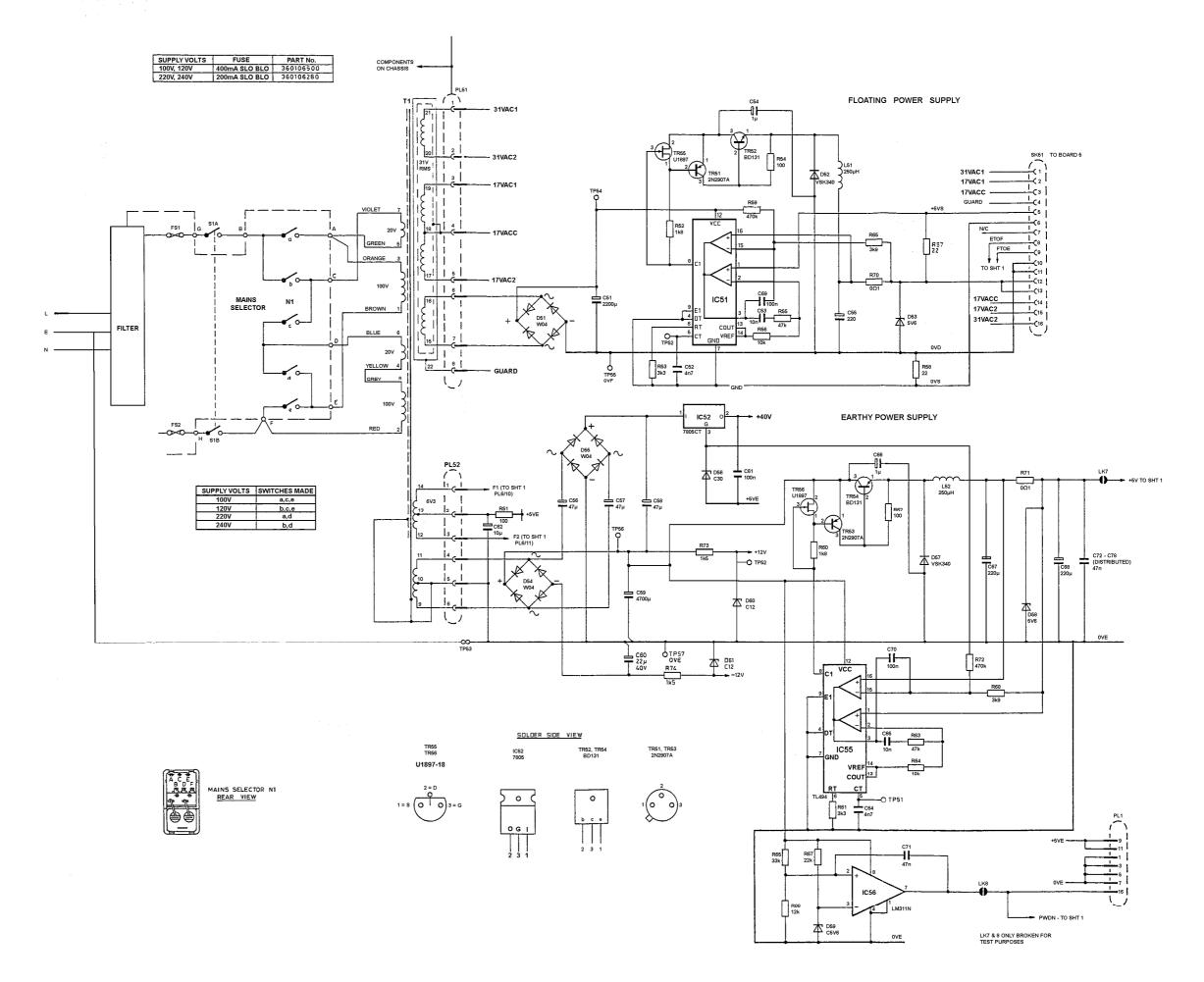
# 7081 General Assembly

Chassis Assembly Part 2 Chassis Assembly Part 1 Front Moulding Assembly Rear Panel Assembly PCB 3 Assembly PCB 5 Assembly Chassis S/Plate Assembly T/Form PCB 3 Lead Mains SKT Lead Brown Mains SKT Lead Blue Screen Transformer	70810002A 70810003A 70810004A 70810005A 70810503X 70810505X 70810208A 70810217A 70810218A 70810219A 70812021A 309617701
Chassis/PCB 5 Lead Cable Clip S/ADH Sleeve, Rubber Black Sleeve, PTFE Natural Sleeving, 4mm Black Cable Assembly, 16-Way Cable Clip S/ADH Display Keyboard Assembly	70810222A 412090440 425100000 429500080 425509000 359900260 412090340 70810006A
Switch Assembly Keyswitch PCB 1 Assembly PCB 4 Assembly PCB 6 Assembly PCB 8 Assembly Cable Assembly	70810207B 377000410 70810501X 70810504X 70810506X 70810508X 35300233A
Socket, 5-way Cover Top Final Assembly Cover Top Assembly Screen Top Cover Screen Insulation Screen Insulation Cover Bottom Final Assembly Cover Bottom Assembly Screen Bottom Assembly Screen Insulation	352105010 70810007A 70810209A 70819510X 70812011A 70812006A 70810008A 70810210A 70810213A 70812020A
Accessories  Rear Panel Assembly  Rear Panel  Input Socket/Board 6	70810009A 70812003A 70810220A
Cable Assembly, RS232 Cable Assembly, Minate Cable Assembly, GP-IB Rear Panel/Trasnformer Lead Socket, 5-way Socket, 5-way DIN Socket, 4-way Mains Switch, DPCO Mains Selector Fuselink, 200mA (for 240v supply) Fuselink, 400mA (for 120v supply)	70810201A 70810202A 70810211A 70810215A 352105010 352505020 352504100 375500030 550001480 360106280
Sleeve, Rubber Black Sleeve, Rubber Black	425100500 425100000

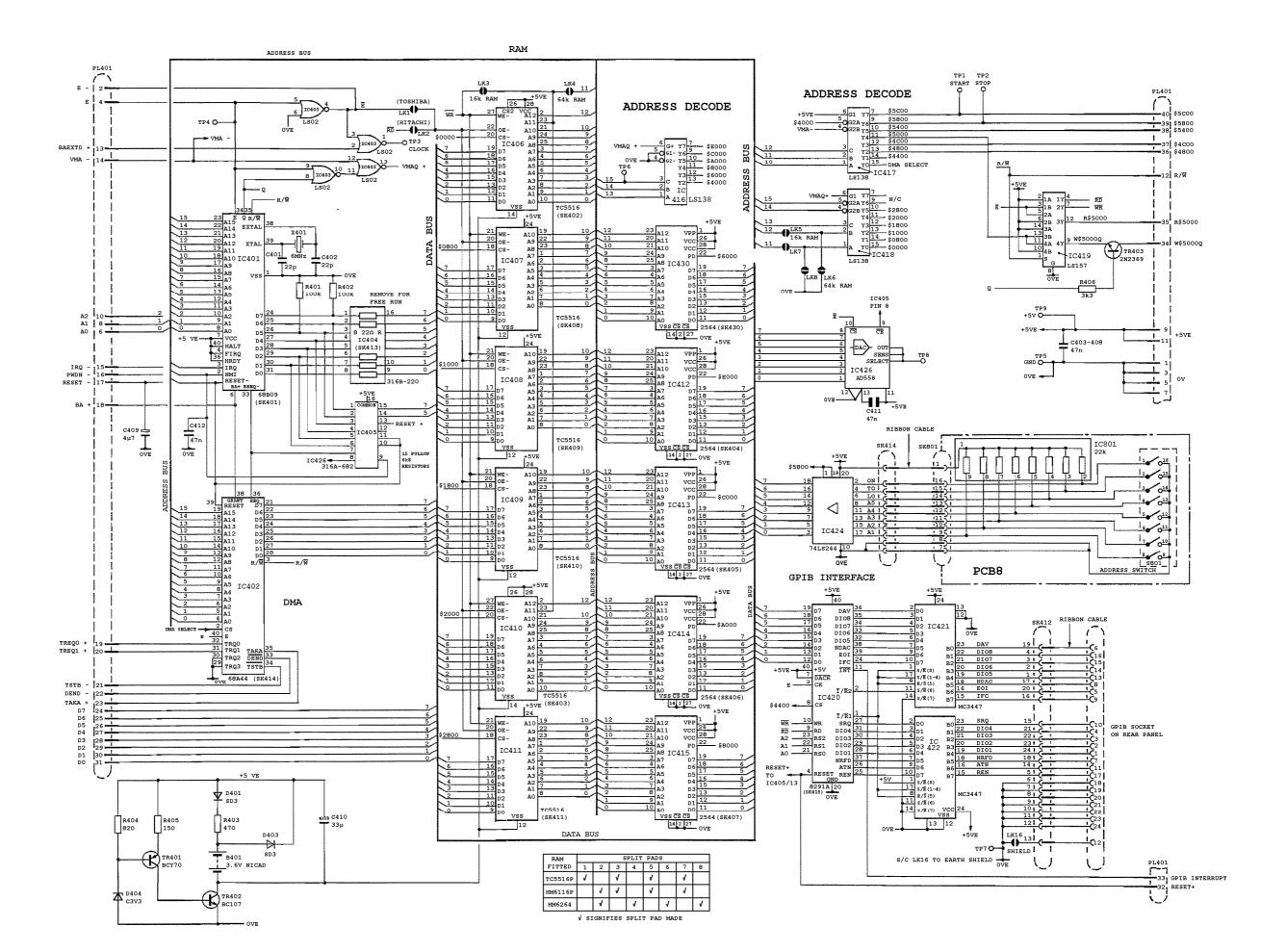
Sleeve, PTFE Natural Sleeving, 4mm Black Resistor, 1M Wire, 7/0.2 PTFE Red Wire, 7/0.2 PTFE Green Wire, 23/0.2 PVC Green/Yellow	429500080 425509000 172361000 480073020 480073050 480095740
Board Interconnection Assemblies Cable Assembly, Boards 5-6 Plug, 34-Way Socket, 34-Way Ribbon Cable, 34-Way	70810206A 351334010 351534010 480095500
Cable Assembly, Boards 5-6 Plug, 10-Way Socket, 10-Way Ribbon Cable, 10-Way	70810205A 351310040 351510060 480095560
Cable Assembly, Boards 3-4 Plug, 40-Way Socket, 40-Way Ribbon Cable, 40-Way	70810204A 351340020 351540010 480120590
Cable Assembly, Boards 1-3 Plug, 26-Way Socket, 26-Way Ribbon Cable, 26-Way	70810203A 351326030 351526020 480095520

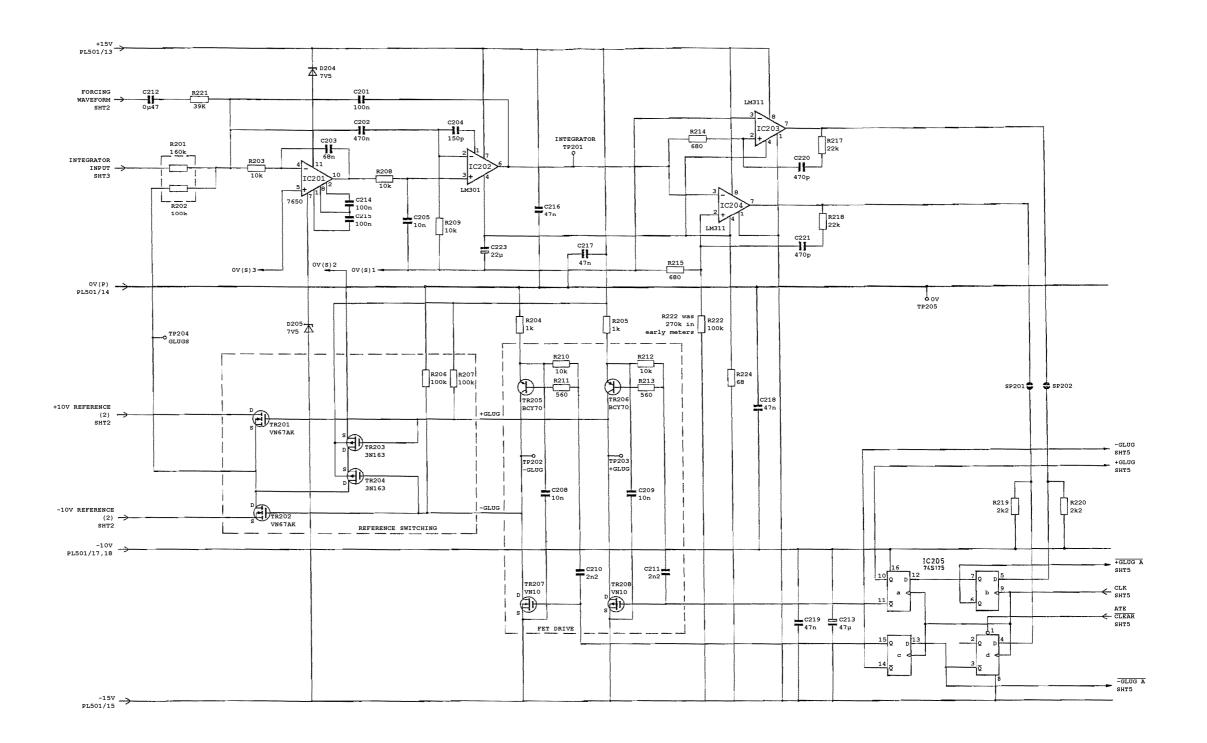


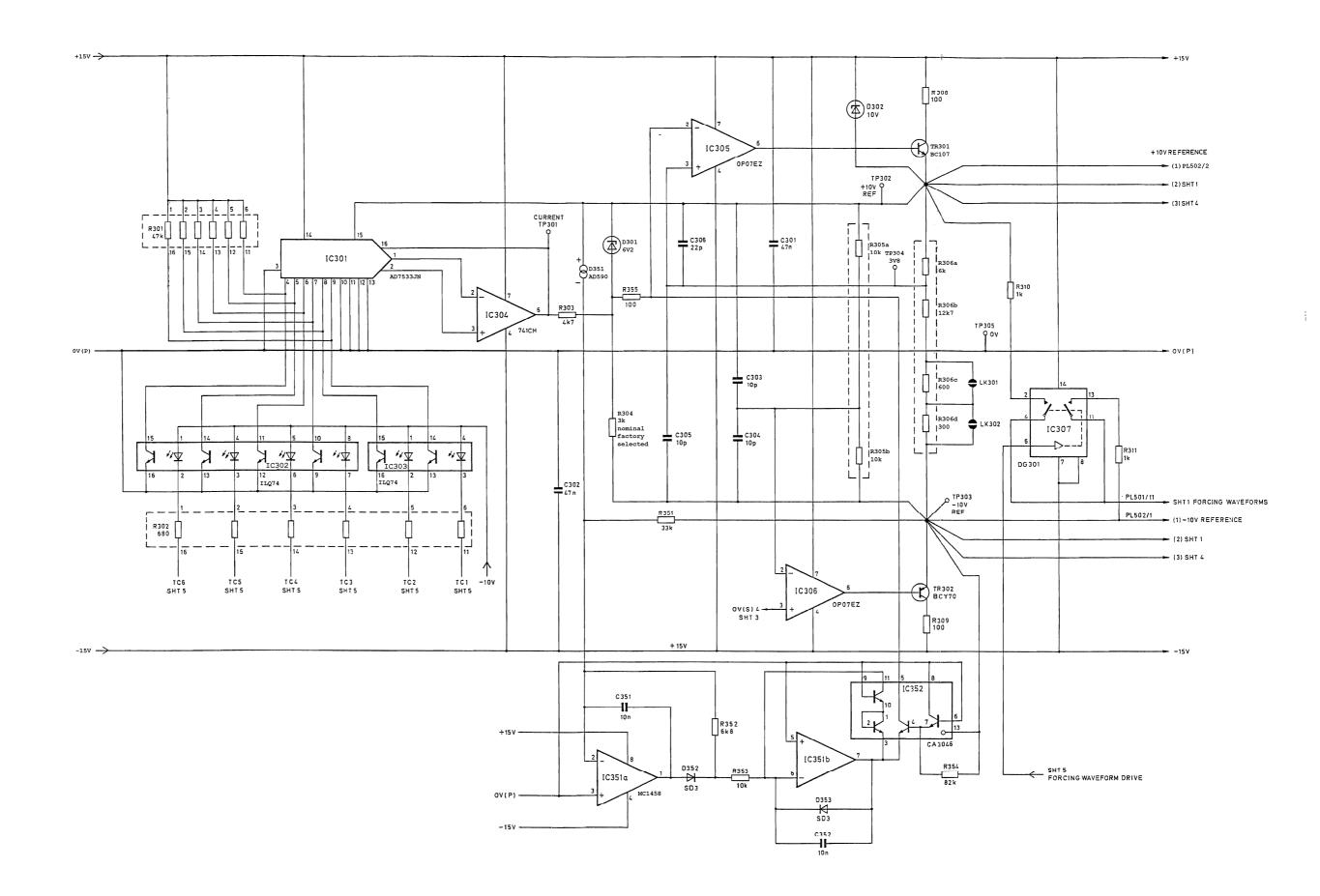


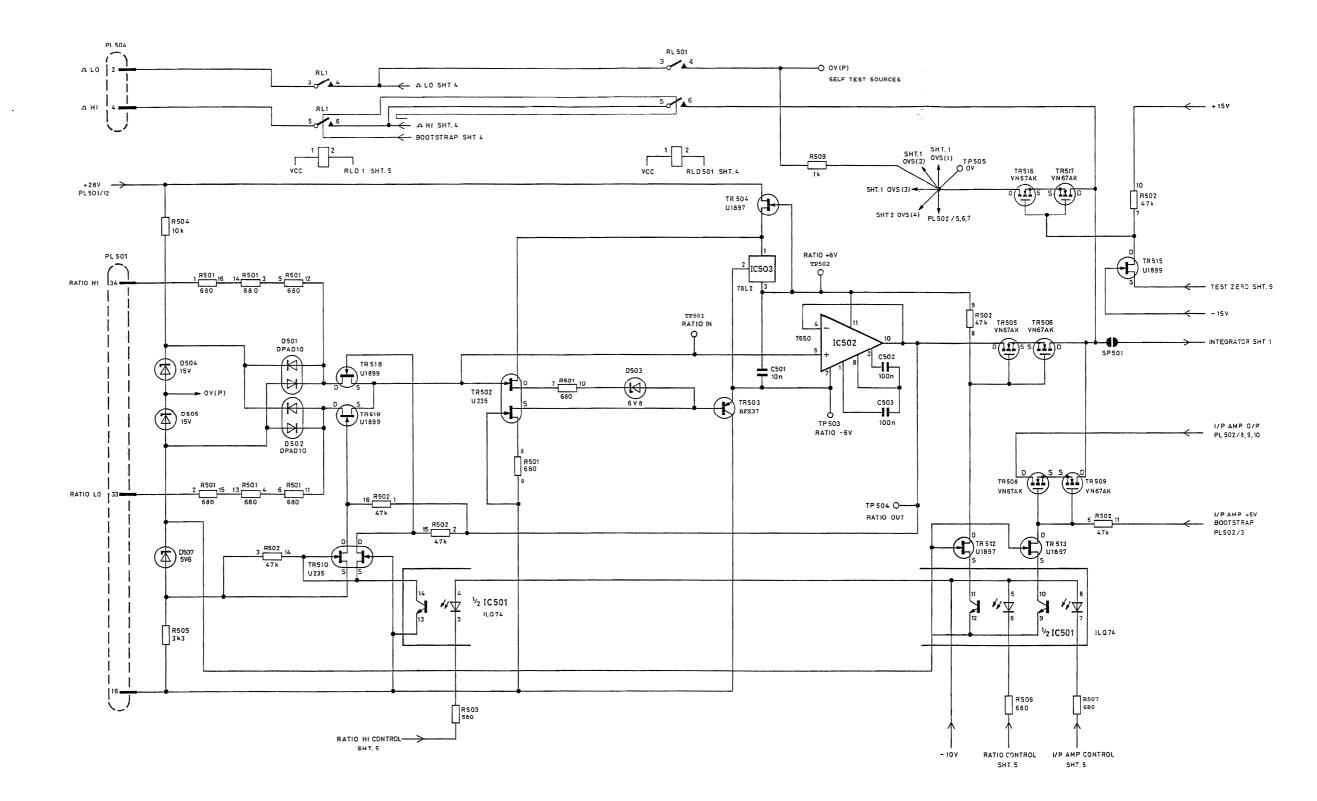


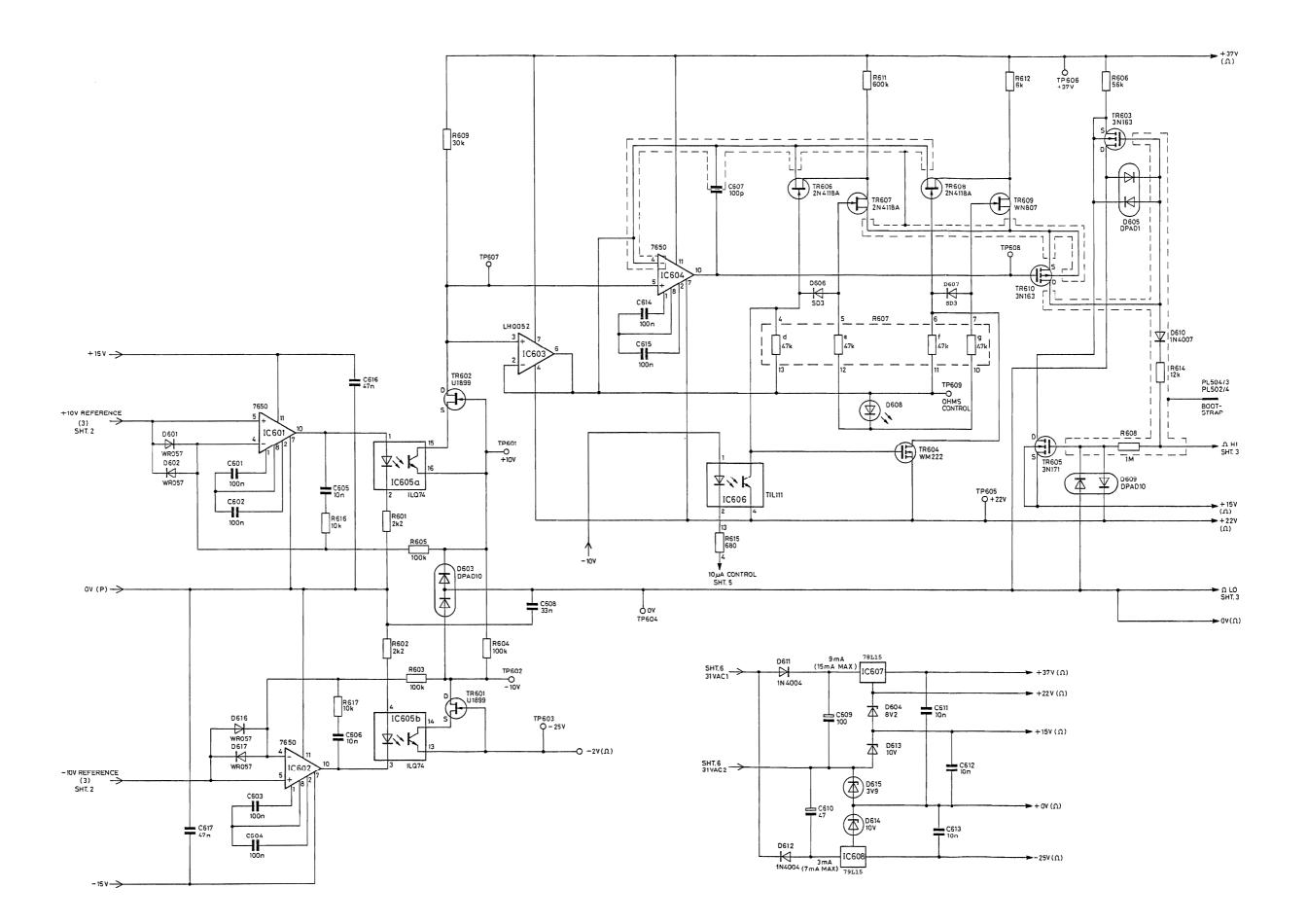
Power Supply (2) 70817503 Sh.2

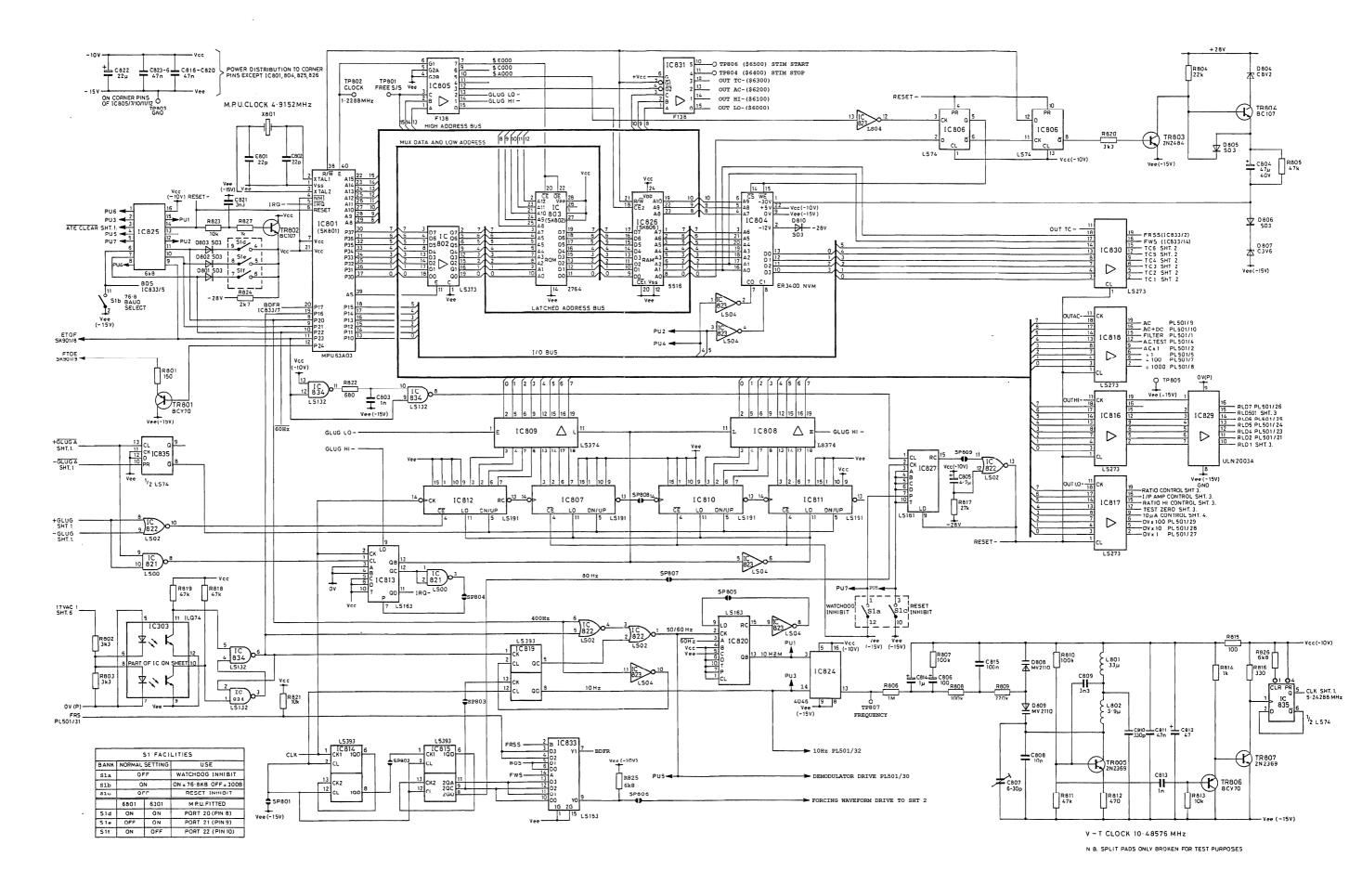




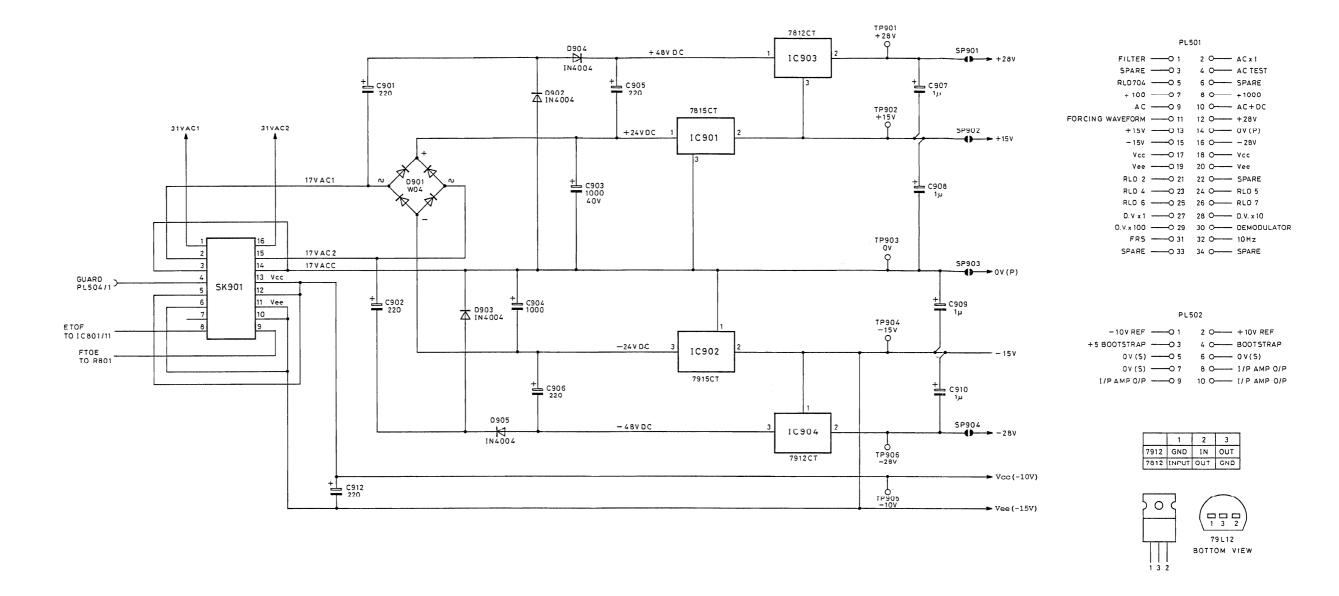


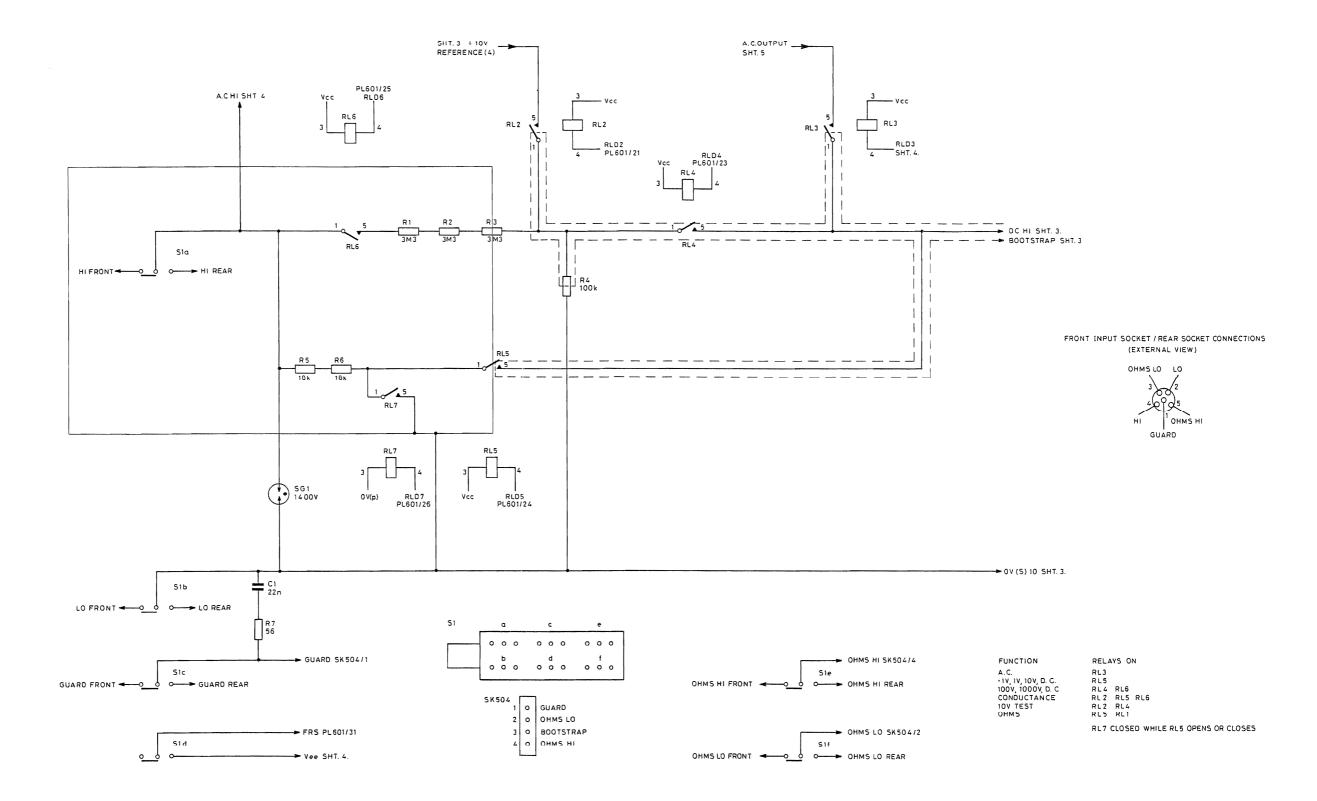


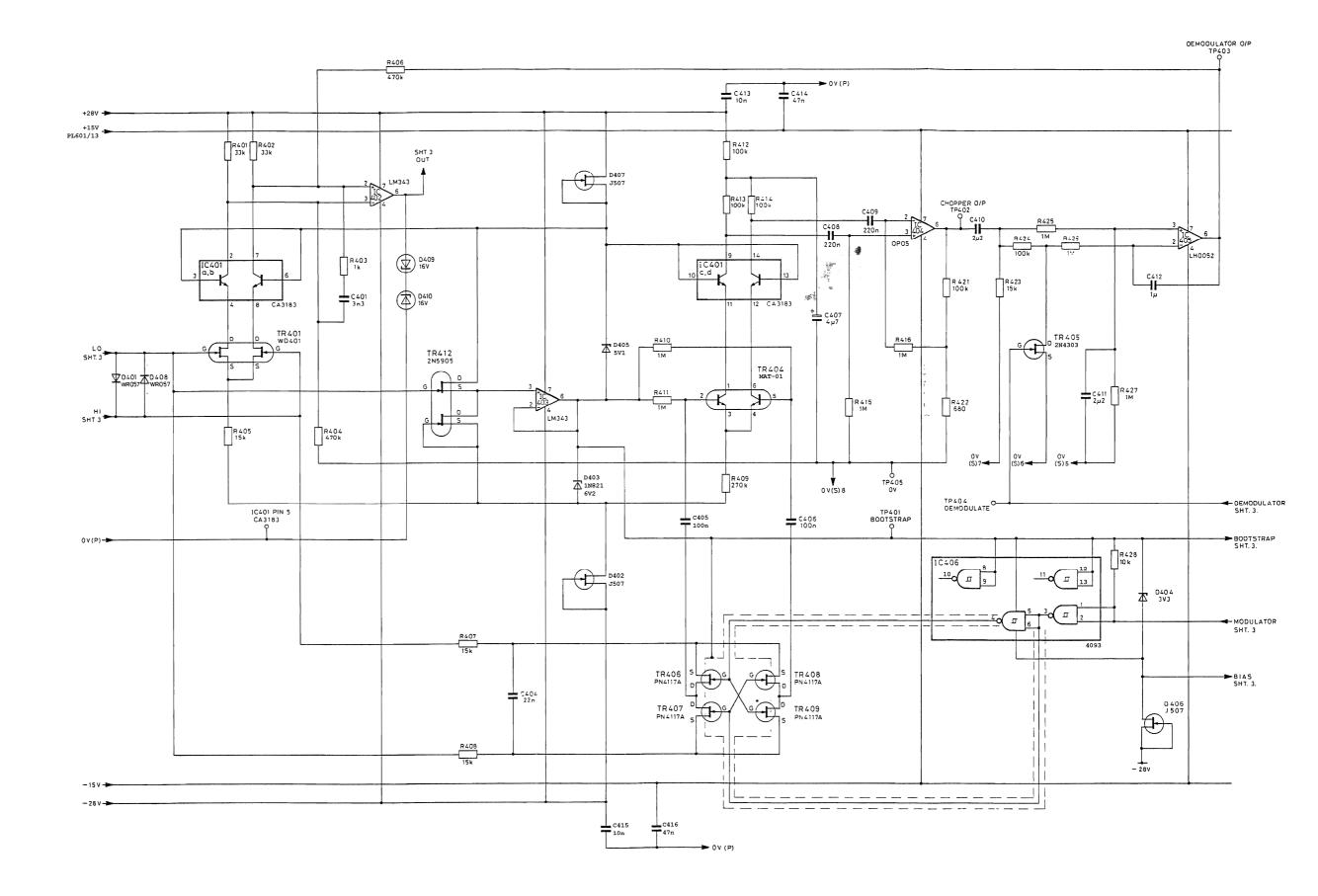


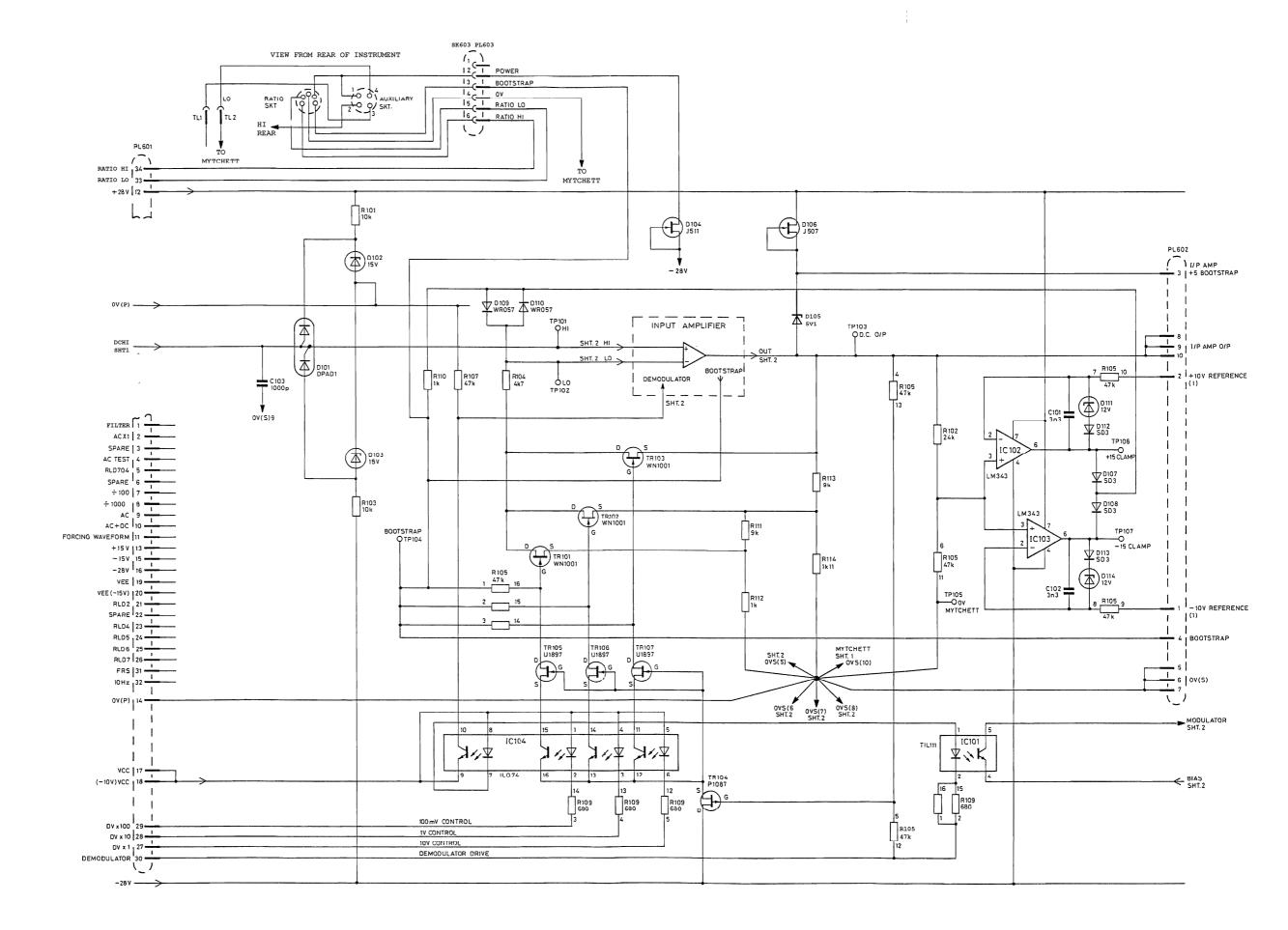


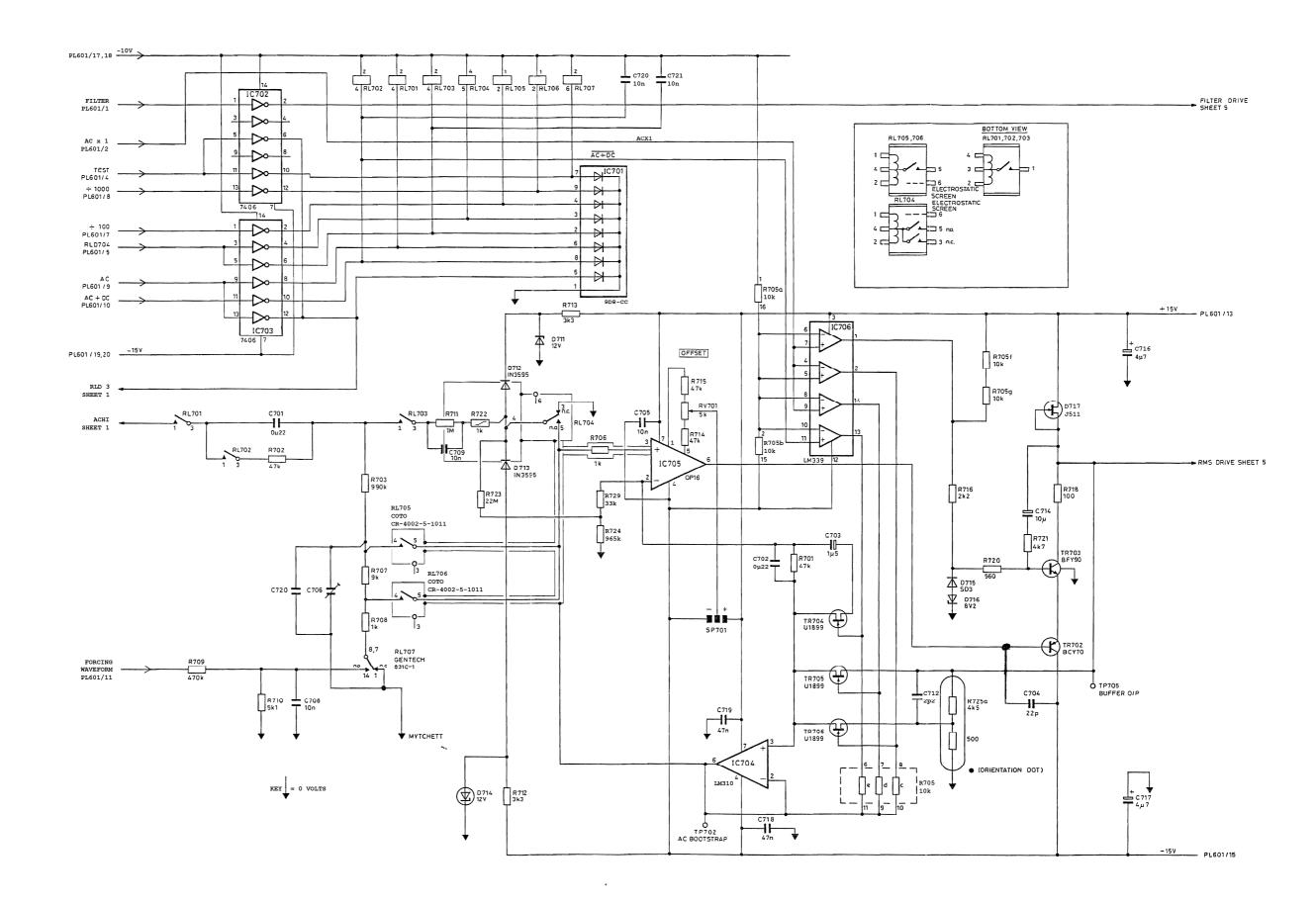
Floating Logic (5) 70817505 Sh.5

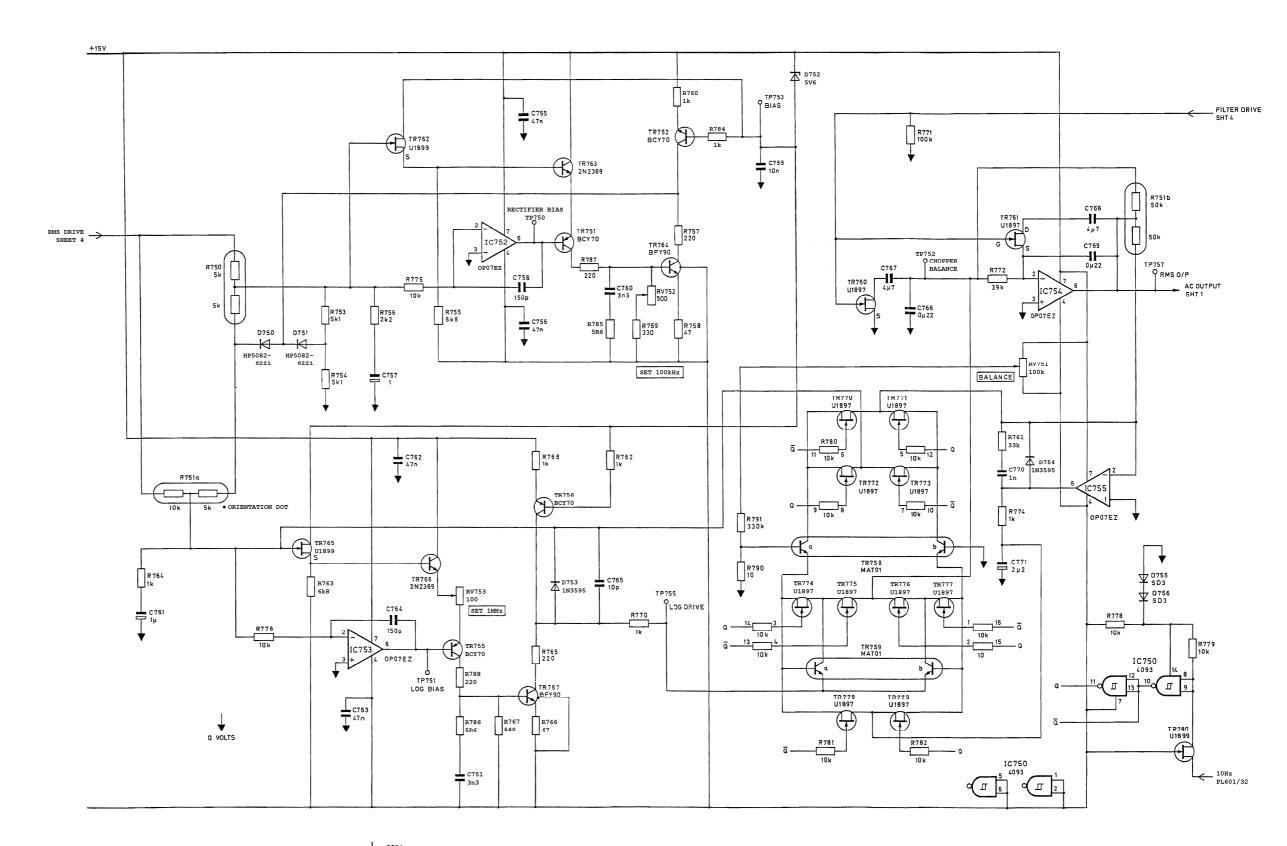


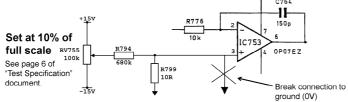




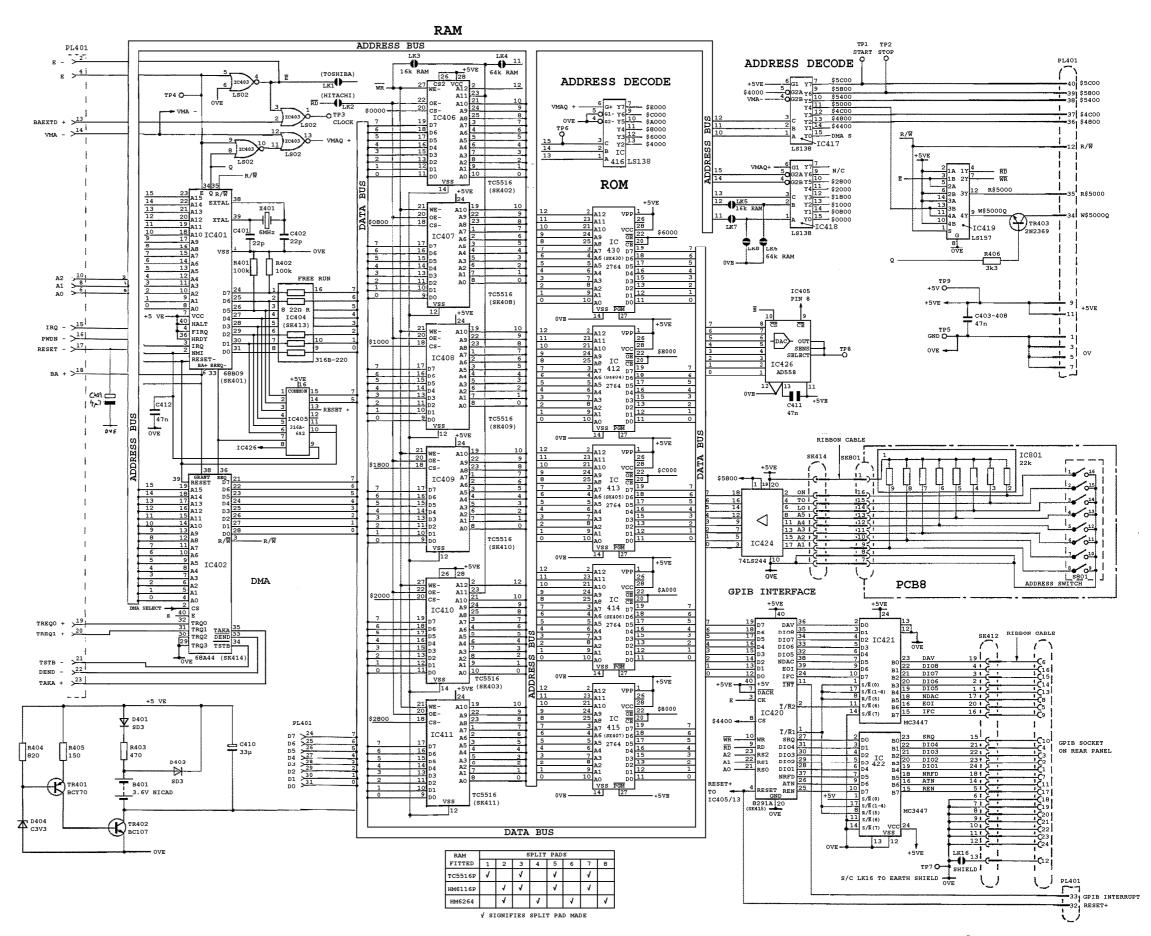




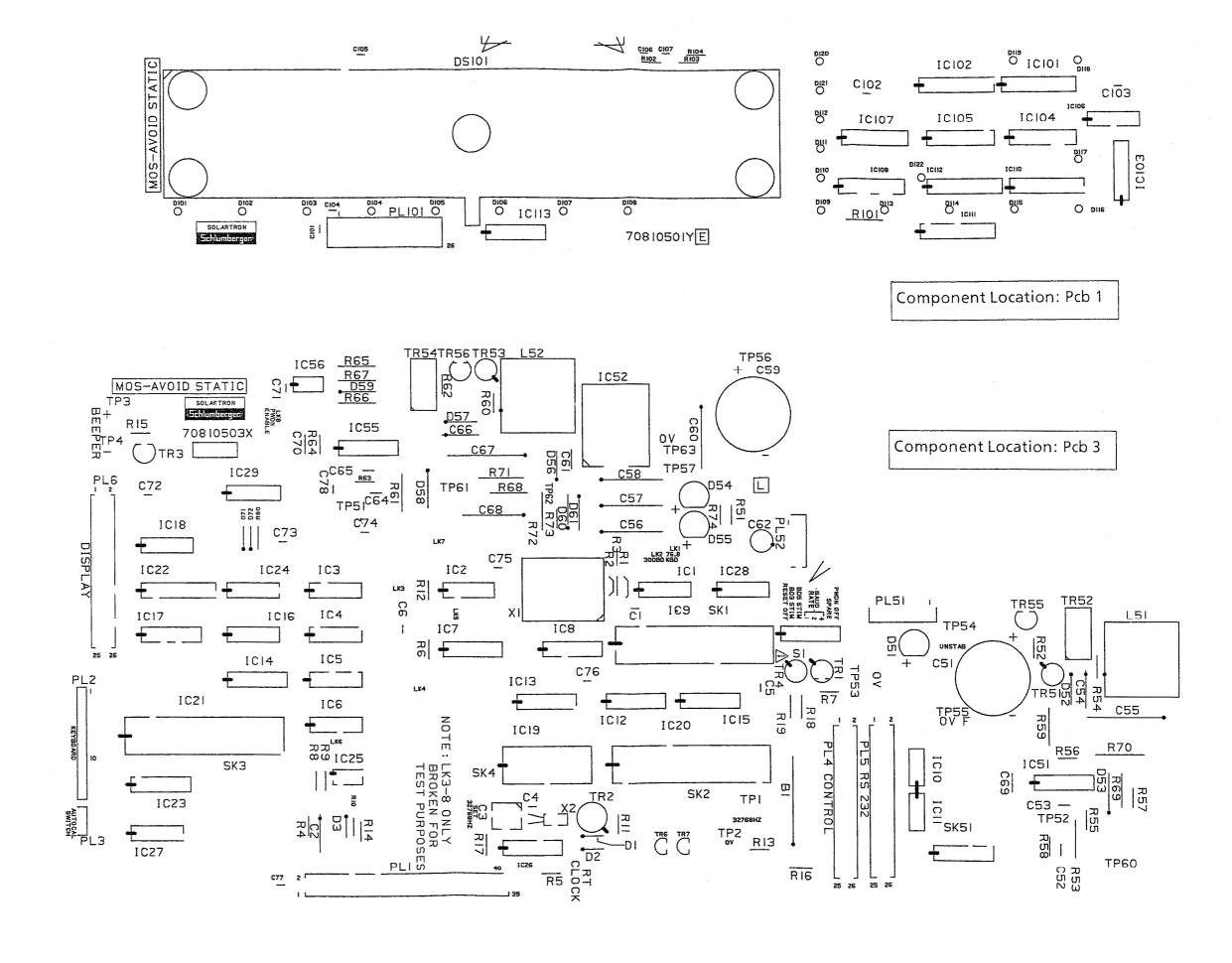


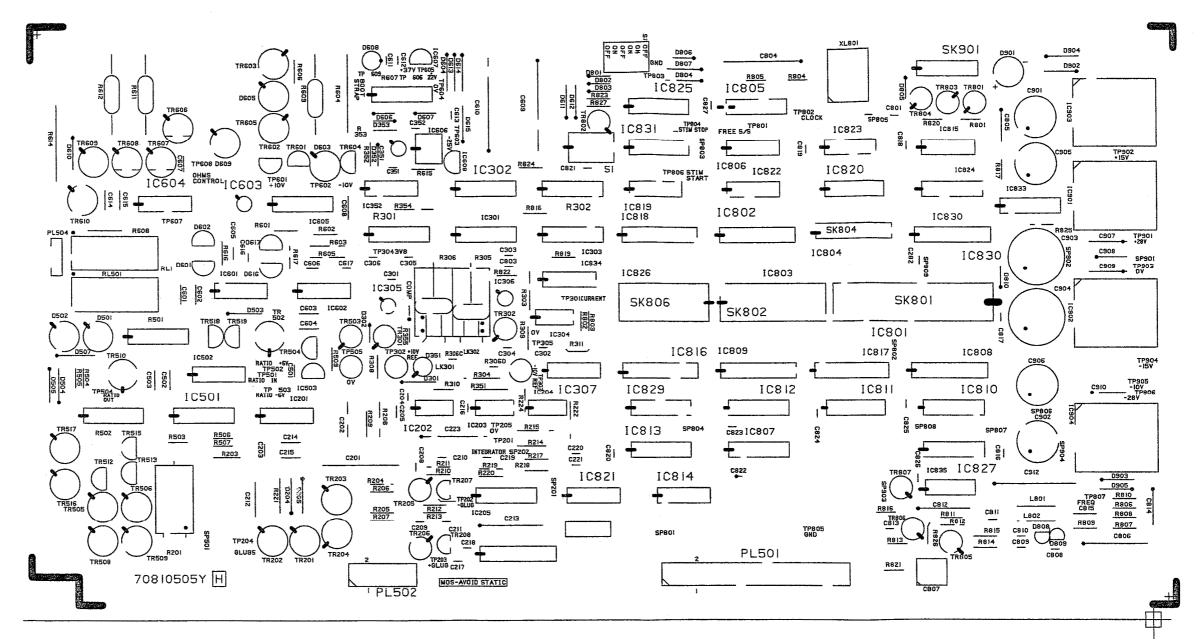


AC Linearity Adjustment Modification made in later meters



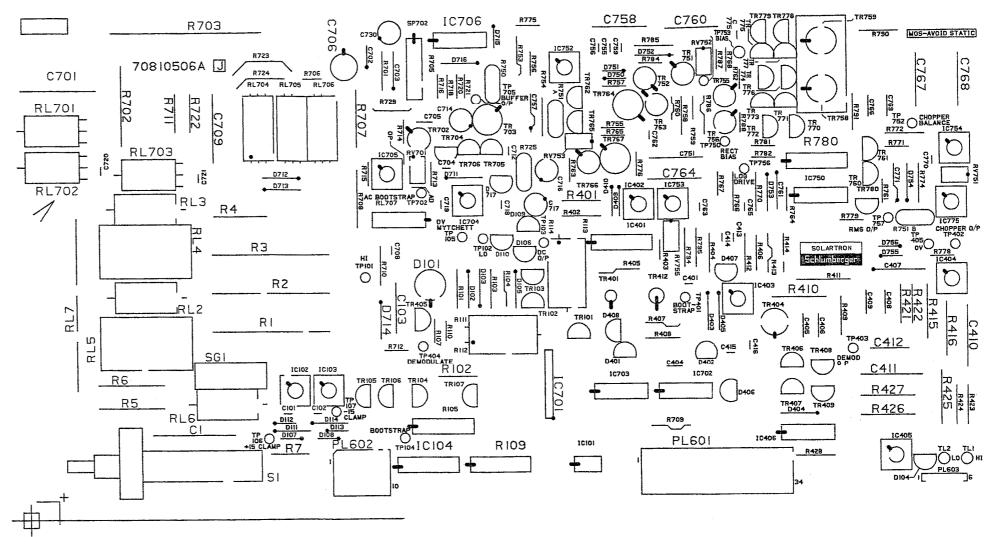
Earthy Processor 70817514/70817508





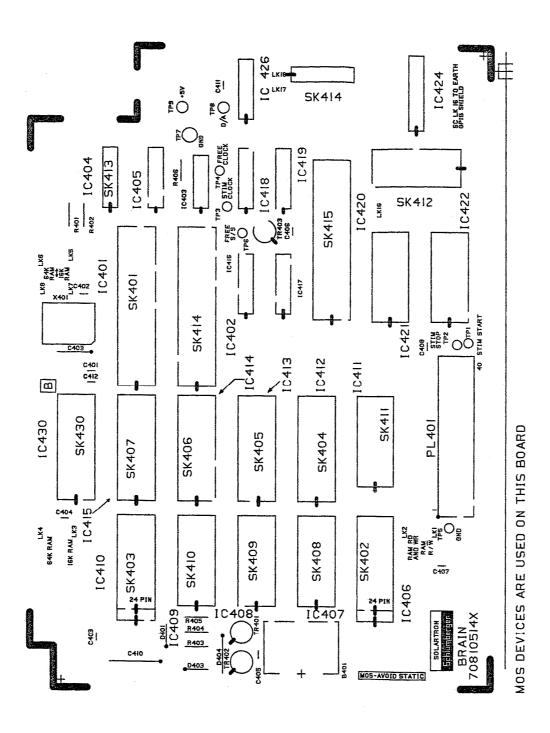
MOS DEVICES USED ON THIS BOARD

70819505 -H NOTATION

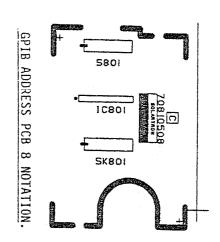


70819506-J MOS DEVICES ARE USED ON THIS BOARD NOTATION

Component Location: Pcb 6



Component Location: Pcb 14



Component Location: Pcb 8

## CHAPTER 8 Montior, Calibration and Self Test

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## 8.1 Monitor Command

The MONITOR command enables the user to access the address/data space of both the "earthy" and "floating" processors of the 7081. The command should only be used by qualified service personnel and requires the use of an RS232 terminal operating at a preferred baud rate of 9600. The Reset Inhibit switches on printed circuit boards 3 and 5 should be set to ON, whilst the MONITOR command is being used, and the baud rate switches set to match the baud rate of the terminal.

- WARNING: 1. The Reset Inhibit switches must be set to OFF when returning from MONITOR, ie, before the instrument undergoes a Device Clear, Power Off/On or Initialise.
  - 2. Great care must be taken when writing data into the unit using the MONITOR command as incorrect use may result in confused operation and/or loss of calibration constants.

## 8.1.1 Earthy Monitor

To access the "earthy" processor, enter:

MONITOR Carriage Return (CR)

The 7081 will respond with:

М

Facilities To inspect an address location, enter:

aaaa,

where aaaa is the address in hexadecimal

The 7081 will respond with the contents on the same line, ie:

M 0000, 07-

To inspect the next location, enter:

To change the existing value, enter:

المحادث فيتنا ليتعرف والسوارة والما

dd. CR

ie; M 0000, 07-08

To inspect a new address, enter:

CR

bbbb,

where bbbb is the new address

To initialise the NVM (Non-Volatile Memory), enter:

## I CR

This command writes a chequer board pattern into the NVM together with a checksum. Any calibration constants present will be lost.

To transfer to the "floating" processor, enter:

## T CR

To exit from MONITOR back to normal operation, enter:

## CTRL X

Note: Any alpha hexadecimal characters must be entered in capitals.

Refer to Table 8.1 for a list of the main address locations for Earthy Monitor.

Table 8.1 Earthy Monitor Address Locations

Location		ss  Software  from AF	Comments
MEMORY	2F1D	2F2E	Used for establishing constant values (see 'Interpreting Data')
	10E0	10F1	Negative acknowledge from floating error counter
	10E2	10F3	Floating to Earthy receive error counter
MAINS FREQUENCY	0F64	0F75	Produces the following possible values:  31 = 50Hz 32 = 60Hz 33 = 400Hz
DUMP OF NVM CONTENTS	1071	1082	Produces the following possible values:  0 = Dump OK 1 = Overrun Error 2 = Underrun Error 3 = Message checksum error
NVM PAGE	1070	1081	Produces the following possible values: 0 = Both pages failed, page 2 used and defaulted where necessary 1 = Page 1 in use 2 = Page 2 in use, page 1 failed
VDC Constants	0F70	0F81	10 constants, ie 5 ranges, 2 constants per range
VAC Constants	0FA2	0FB3	5 constants, ie 5 ranges, l constant per range

Location		s Software from AF	Comments
Ohms Constants	0FBB	0FCC	10 constants, ie 5 ranges, 2 constants per range
Top Ohms Range Constants	OFED	OFFE	3 constants, ie l range, 3 constants
Ratio Input Constants	0FFC	100D	l constant, ie l range, l constant
Zener Temp- erature coefficient	·106E	107F	
Page Checksum	106F	1080	

## 8.1.2 Floating Monitor

Access to the "floating" processor is only possible via the "earthy" processor. (See previous section).

Once the transfer command has been entered, the unit will respond with the sign on message "DIS EM FLOAT" followed by the prompt !, indicating that the unit is in the RAM/ROM mode.

Two modes are possible:

\* To change to RAM/ROM mode, enter:-

R CR

The 7081 will respond with:-

!

\* To change to NVM mode, enter:-

N CR

The 7081 will respond with:-

Facilities To inspect an address location, enter:

aaaa

where aaaa is the address in hexadecimal.

To change the value, enter:-

dd CR

Note: If the NVM mode is enabled, addresses 0 to 3FF only have any meaning.

To print a block of memory, enter:

P SSSS, FFFF

where SSSS, is the start address in hexadecimal and FFFF is the end address in hexadecimal e.g.

"PO,AO

0000 0A 05 .....

0010 0A 05 .....

0020 0A 05 .....

0030 0A 05 .....

0040 0A 05 .....

0050 0A 05 .....

0060 0A 05 .....

0070 0A 05 .....

0080 0A 05 .....

0090 0A 05 .....

0000 0A 05 .....

To return to the "earthy" processor, enter:-

CTRL X

WARNING: Writing to the NVM will destroy the calibration constants.

Refer to Table 8.2 for a list of the main address locations for Floating Monitor.

Table 8.2 Floating Monitor Address Locations

Location		s Software from AF	Comments
Link Receiver Error Counter	0068	002E	Earthy to Floating link receive error counter.
Link Transmit Error Counter	0084	0030	Floating to Earthy Link counter
ROM Ident		FFDA	· :

8.1.3 Interpreting Calibration Constant Data Each calibration constant consists of a packed binary number of 5 bytes in the following form:-

Byte No. 0 1 2 3 4
sign bit 7 bit 2's 32 bit mantissa complement exponent

The easiest way to interpret the value of a constant is to write the number into the 7081 memory, come out of monitor, turn on the RS232 output and type MEMORY? The value will be output at the terminal in engineering format. For example:

```
M 0F70,71-,AA-,80-,00-,00-

M 2F1D,00-71,18-AA,0A-80,18-00,00-00

M

OUT,RS232,ON

OK

MEM?

OK

Memory contents = 20.3251838E-06
```

When inspecting the NVM, each location is only a nibble wide. Therefore, each constant occupies ten locations not five as in the RAM copy on the "earthy" side. The NVM has two identical pages: locations 0 to lFF are page 1 and locations 200 to 3FF page 2. In order to interpret a number it is first necessary to reform the bytes from the nibbles. The first nibble of a byte pair is the most significant nibble, the second nibble the least significant. Once reformed the five byte number can be put into the memory as before, e.g.

```
M T
* DIS EM FLOAT *
!N
"0,07-,01-,0A-,0A-,08-,00-,00-,00-,00-,00-
M 2FlD,00-71,18-AA,0A-80,18-00,00-00

M
OUT,RS232,ON
OK
MEM?
OK
Memory contents = 20.3251838E-06
```

Constants are given in ascending range, all the constants for each range being grouped together in the order (where applicable) of Zero, High, Open.

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## 8.2 Calibration Messages

The responses to the CALIBRATE? command are described below. Reference should also be made to the MONITOR command for a further breakdown.

- FAIL 1 this message is output if the checksum in page 1 and/or page 2 of the NVM has failed. It is equivalent to the front panel 'NVM FAIL' message, which could appear at power up.
- FAIL 2 if a failure occurs during the transfer of the calibration constants from the NVM to the RAM, this message is output. It is equivalent to the front panel 'DUMP FAIL' message, which could appear at power up.
- FAIL 3 this message is output if some of the calibration constants are out of range and default values have been susbstituted. It is equivalent to the front panel 'CAL INCOMPLETE' message, which could appear at power up.
- OK if this message is output, the transfer of the calibration constants has been successfully completed and no errors have been found.

#### 8.3 Calibration Commands

Two commands are provided to enable inspection or refresh of the unit calibration constants. They can both be activated via the RS232 or GP-IB interfaces.

#### 8.3.1 CALIBRATE, DUMP

This command enables an output of all the calibration constants, with headings, and the zener temperature coefficient current token.

To activate a calibration dump, the following procedure should be used. (It is assumed that an RS232 terminal is connected to the voltmeter).

- \* Turn the front panel calibration key to the CAL position.
- \* Enter,

Output,RS232,ON

CALIBRATE, DUMP

\* The voltmeter will respond with the output shown in Figure 8.1.

```
VDC CALIBRATION CONSTANTS
 8.04662704E-06
 164.224612E-03
-834,465026E-09
1.64196003E+00
-953.674316E-09
 16.4218391E+00
-298.023223E-09
164.185607E+00
-774.860382E-09
1.64381286E+03
VAC CALIBRATION CONSTANTS
327.550067E-03
 3.27523722E+00
 32.7807025E+00
 328,446396E+00
 3.29051217E+03
KOHM CALIBRATION CONSTANTS
 8.04662704E-06
165.944119E-03
-834.465026E-09
 1.65961519E+00
-953.674316E-09
16.5984867E+00
-834.465026E-09
165.980795E+00
-953.674316E-09
 1.66008452E+03
TOP OHMS RANGE CALIBRATION CONSTANTS
-953.674316E-09
 9.90188959E+03
 602.393984E-03
RATIO TERMINALS CALIBRATION CONSTANT
 16.4375923E+00
ZENER CURRENT TOKEN VALUE
068
```

Fig. 8.1 CALIBRATE, DUMP Output

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Vdc Calibration Constants These constants are given in the following order: 0.1 Volt range zero, 0.1 Volt range high, 1.0 Volt range zero, 1.0 Volt range high, etc., up to 1000 Volt range high. The values take into account the range factor and the digital full scale constant value of 16777216. As the 7081 is designed to produce slightly high results before calibration, the high constants are slightly less than the full scale value, i.e. 1.0Volt range high = 1.64196003, 10 Volt range high = 16.4218391, etc.

Vac Calibration Constants The Vac mode has high calibration constants only, given in the order: 0.1 Volt range, 1.0 Volt range, etc., up to 1000 Volt range. The constants are measured at half the full scale value and so are equal to twice the nominal values expected, i.e. 1.0 Volt range constant =  $3.27523722 \text{ which is approximately equal to } 1.64 \times 2.$ 

Kohms Calibration Constants These constants appear in the following order: 0.1k ohms range zero, 0.1k ohms range high, 1.0k ohms range zero, 1.0k ohms range high, etc., up to 1000k ohms range high. The zero constants are obtained from the Volts dc set according to the range on which the ohms measurement is taken. The zero constants are transferred to the k ohms set when an NVM dump is performed.

Top Ohms Constants The three constants for the M ohms range are given in the order: zero, open, high. The zero is taken from the 1000k ohm range and the open value is derived from the reference circuit.

Ratio Constant The Ratio has a calibration high constant but no zero as any zero offsets in the circuit would be cancelled out by the subtraction of Ratio Lo from Ratio Hi. The constant is measured on the Ratio 10 Volts range.

Zener Current Token Value This value represents the code sent by the microprocessor to set up the reference zener current. It is designed to give the diode the lowest temperature coefficient.

## 8.3.2 CALIBRATE, REFRESH

This command enables a refresh of the NVM, i.e. the present calibration constants are written back into the NVM. The sequence of operation is as follows:

- \* Microprocessor checks both pages of the NVM.
- \* First correct page is down-loaded\_to-the RAM. -
- \* Microprocessor checks the RAM
- \* RAM contents are written into both pages of the NVM.
- \* Microprocessor checks both pages of the NVM.

To activate a calibration constants refresh, the following procedure should be adopted. (It is again assumed that an RS232 terminal is connected to the voltmeter).

\* Turn the front panel calibration key to the CAL position.

- \* Enter, Output,RS232,ON CALIBRATE,REFRESH
- \* One of the following messages will appear:

REFRESH COMPLETE - refresh has been successful and no faults have been found.

REFRESH COMPLETE NVM PAGE 1 WAS FAULTY

- refresh has been successful. Page 1 of the NVM was originally faulty but is now correct.

REFRESH COMPLETE NVM PAGE 2 WAS FAULTY

 refresh has been successful. Page 2 of the NVM was originally faulty but is now correct.

REFRESH FAIL RAM COPY FAIL

- refresh has been unsuccessful as the RAM copy is faulty.

REFRESH FAIL NVM PAGE 1 IS FAULTY

 refresh has been unsuccessful. Page 1 of the NVM is faulty.

REFRESH FAIL NVM PAGE 2 IS FAULTY

- refresh has been unsuccessful. Page 2 of the NVM is faulty.

REFRESH FAIL NVM PAGE 1 & 2 ARE FAULTY

- refresh has been unsuccessful. Both pages of the NVM are faulty.

Note: The 7081 display outputs either REFRESH COMPLETE or REFRESH FAIL.

## 8.4 7081 Calibration

The 7081 is sent from the factory in a fully calibrated state but, if the unit is damaged or the specifications exceeded, re-calibration may be required. Owing to the high accuracy of 7081, the calibration reference values entered should be very precise. Solartron will re-calibrate the unit if the user is unable to supply precise references.

Note: All calibration should be performed in a stable temperature environment, i.e. variation of less than  $\pm 1$ °C.

## 8.4.1 Complete Re-calibration

If a new Non-Volatile Memory (NVM) is installed in the unit, it is necessary to perform a complete re-calibration of 7081 using the procedure given below.

It is assumed that an RS232 terminal device is connected to the 7081.

- \* With reference to Section 8.1, set the Reset Inhibit switches to ON and initialise the NVM.
- \* Exit from MONITOR and set the Reset Inhibit switches to OFF.
- \* Turn the front panel key operated switch to the CAL position.
- \* Insert a short circuit plug into the input socket and enter the following command:

CALIBRATE, VDC=0.1, ZERO

- \* Wait a few seconds for the unit to complete the 'zero' calibration, then remove the short circuit plug and connect a reference supply of approximately 0.1 volts dc to the input.
- \* Enter:

CALIBRATED, VDC=0.1, HIGH=0.100012

where 0.10012 is the 'exact' value of the reference supply.

- \* Repeat the previous three steps for each of the volts dc ranges, using a suitable reference input.
- \* Connect an ac reference supply of approximately 0.1 volts to the input.
- \* Enter:

CALIBRATE, VAC=0.1, HIGH=0.100012

where 0.10012 is the 'exact' value of the reference supply.

- \* Repeat these two steps for each of the volts ac ranges, using a suitable reference input.
- \* Remove the input lead and leave the input open circuit.
- \* Enter:

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CALIBRATE, KOHM = 10000, OPEN

- \* Wait a few seconds for the unit to complete the 'open' calibration, then connect a reference supply of approximately 10000 kohms to the input.
- \* Enter:

CALIBRATE, KOHM = 10000, HIGH = 10000

where 10000 is the 'exact' value of the reference.

\* Connect a reference supply of approximately 1000 kohms to the input and enter:

CALIBRATE, KOHM = 1000, HIGH = 1000

where 1000 is the 'exact' value of the reference.

- \* Repeat the previous step for each of the remaining kohms ranges, using a suitable reference input.
- \* Connect a reference supply of approximately 10 volts dc to the input. to the ratio reference input on the rear panel (This step performs the RATIO calibration)

\* Enter:

CALIBRATE, REFERENCE, HIGH = 10.000012

where 10.000012 is the 'exact' value of the reference.

\* Do <u>not</u> attempt to re-calibrate the zener diode. Refer to Solartron.

## 8.4.2 Partial Re-calibration

If a particular range or mode requires re-calibration, it is recommended that the NVM first be refreshed using the procedure set out in Section 8.3.2. The range/mode can then be re-calibrated as described in the previous section.

Whenever calibration is being carried out, reference should be made to the CALIBRATE command described in Chapter 3, of 7081 Operating Manual, Part 2.

## 8.4.3 GP-IB Calibration Program

When calibrating the 7081 over the GP-IB a program is required which (a) commands the 7081 to calibrate the necessary ranges/modes and (b) tells the operator when to connect the reference supplies, etc. The following example program, written in HP9835A Basic, calibrates the 10 Volts dc range and could be adapted or expanded for other modes/ranges. To use a program of this type, the controller must be able to perform both a parallel and a serial poll.

- 10 !EXAMPLE CALIBRATION OF 7081
- 20 !set up program parameters
- 30 S=0
- 40 P=0
- 50 Waiting=0
- 60 Signal=0
- 70 Rqs=6
- 80 Rdy=4
- 90 !INITIALISE 7081
- 100 RESET 716
- 110 OUTPUT 716; "INITIALISE"
- 120 WAIT 3000
- 130 GOSUB Setremote
- 140 PRINT "TURN KEY TO CAL ON 7081"
- 150 DISP "PRESS CONTINUE WHEN READY"
- 160 PAUSE
- 170 ON INT#7 GOSUB Intserve

```
180 CONTROL MASK 7:128
190 CARD ENABLE 7
200 OUTPUT 716; "CALIBRATE, REFRESH"
210 OUTPUT 716; "SRQ, READY, ON"
220 Signal=0
230 GOSUB Waitsignal! WAIT FOR REFRESH END
240 OUTPUT 716; "SRQ, OFF"
250 PRINT"
                               CALIBRATE.VDC, 10, ZERO"
260 GOSUB Shortcircuit
270 OUTPUT 716; "CALIBRATE, VDC, 10, ZERO"
280 OUTPUT 716; "SRQ, READY, ON"
290 GOSUB Waitsignal! WAIT FOR COMPLETION
300 OUTPUT 716; "SRQ, OFF"
310 PRINT"
                               CALIBRATE, VDC, 10, HIGH=[ref.value]"
320 GOSUB Connect
330 OUTPUT 716; "CALIBRATE, VDC, 10, HIGH=10.0"
340 OUTPUT 716; "SRQ, READY, ON"
350 GOSUB Waitsignal! WAIT FOR COMPLETION
360 OUTPUT 716: "SRO.OFF"
370 DISP"10VDC RANGE CALIBRATION COMPLETE"
380 STOP
390 Shortcircuit:!
400 PRINT"INSERT SHORTING PLUG INTO 7081 INPUT"
410 DISP"PRESS CONTINUE WHEN READY"
420 PAUSE
430 RETURN
440 Connect:!
450 PRINT"CONNECT REFERENCE TO 7081 INPUT"
460 DISP"PRESS CONTINUE WHEN READY"
470 PAUSE
480 RETURN
490 Setremote:!
500 Remote=1
510 REMOTE 716
520 LOCAL LOCKOUT 7
530 RETURN
540 Intserve:!
550 Int=Int+1
560 PRINT"INTERRUPT#"; Int
570 PPOLL CONFIGURE 716; "00001011"
580 P=PPOLL (7)
590 GOSUB Remotelocal
600 IF BIT(P,3)<>1 THEN GOTO Endpol
610 STATUS 716;S
620 IF BIT(S,Rqs)<>1 THEN GOTO Endpol
630 IF BIT(S,Rdy)=1 THEN GOTO Endtry
640 Signal=1
650 Waiting=0
660 Endtry:!
670 Endpol:!
680 PPOLL UNCONFIGURE 716
690 GOSUB Remotelocal
700 CARD ENABLE 7
710 RETURN
```

720 Waitsignal:!

```
730 Waiting=1
740 Idle=0
750 Repeatwait:!
760 Idle=Idle+1
770 DISP "Status: Waiting for interrupt"; Idle
780 IF Signal=0 THEN GOTO Repeatwait
790 Signal=0
800 PRINT " "
810 RETURN
820 Remotelocal:!
830 IF Remote=0 THEN GOTO Elseremote
840 GOSUB Setremote
850 GOTO Endremote
860 Elseremote:!
870 GOSUB Setlocal
880 Endremote:!
890 RETURN
900 Setlocal:!
910 Remote=0
920 LOCAL 7
930 RETURN
940 END
```

Lines 10 to 80 - set up the program parameters, i.e. serial poll and parallel poll registers, waiting flag for the background routine, interrupt acknowledge flag and serial poll bits.

Lines 90 to 130 - initialise the 7081 and set it to remote.

Lines 140 to 380 - calibrate the 10 Volts dc range.

Lines 390 to 430 - 'Shortcircuit' subroutine to tell the operator to insert the shorting plug.

Lines 440 to 380 - 'Connect' subroutine to tell the operator to connect the reference supply.

Lines 490 to 530 - 'Setremote' subroutine to put 7081 into remote.

Lines 540 - 710 - 'Intserve' subroutine for servicing interrupts.

Lines 720 to 810 ~ 'Waitsignal' subroutine which is a background routine used when the controller is waiting for 7081 to produce interrupts.

Lines 820 to 890 - 'Remotelocal' subroutine which decides if 7081 was in remote or local and returns to its previous state.

Lines 900 to 940 - 'Setlocal' subroutine which sets 7081 to local.

#### 8.5 Self Test

If 7081 fails the self test, initiated by either pressing the front panel self test control or sending the Test command via one of the interfaces, the area of failure can be investigated using the MODE Command.

MODe, TEST Ovdc - measures the integrator zero and outputs the results.

MODe, TEST 10vdc - measures the reference voltage. A value of approximately 10 volts should be output. Values in the region of 9.8 to 10.2 volts are acceptable.

MODe, TEST Kohm - measures a resistor in the V-to-T converter circuit. A value of 166 Kohms should be output.

MODe, TEST Ac - the reference forcing waveform is attenuated to a 100mV square wave and passed through the ac circuitry. Readings of 100mV ± 10% should be

obtained if the circuits are operating correctly.

# CHAPTER 9 Setting Up Procedure

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#### 9.1 Introduction

This chapter provides a comprehensive setting-up procedure which may be necessary after rectification and/or component replacement on the voltmeter.

## 9.2 Test Equipment

The test equipment listed below should be available to carry out setting-up procedures.

- (a) Oscilloscope (20MHz bandwidth)
- (b) Digital Voltmeter (eg Type 7060)
- (c) Calibrator
- (d) Variac Transformer
- (e) Silent 700 (or similar RS232 terminal)
- (f) RS232 Cable
  (g) Frequency Counter (e.g. HP5135A)
  (h) 240V/400Hz Power Supply Unit

## 9.3 Safety

The instrument should be disconnected from the mains supply before any attempt is made to remove the printed circuit boards.

## 9.4 Printed Circuit Board 4 Test

Ensure that the following links are fitted depending upon the RAM used:-

RAM	1	2	3	4	5	6	7	.8	16
5516/6117	In	Out	In	Out	In	Out	In	Out	Out
6116	Out	In	In	Out	In	Out	In	Out	Out
6264	Out	In	Out	In	Out	In	Out	In	Out

Check that the printed circuit board is correctly connected to the following:-

Printed Circuit Board 3 via PL1 GP-IB Socket via SK412

Printed Circuit Board 8 via SK414.

- Switch on the voltmeter and check that "INITIALISED" appears in the display.
- Switch off and then on again, and check that "RESUMED" appears in the display. (This assumes a fully calibrated printed circuit board 5).
- Press the front panel "initialise" control and check that "INITIALISED" appears in the display.
- Set the GP-IB address switch to address 7. Switch off and then on . again, and press the "local" control. "GP-IB ADDRESS=7" should appear in the display.

- \* Set the address switch to address 16. Switch off and then on again, and press the "local" control. "GP-IB ADDRESS = 16" should appear in the display.
- 9.5 Printed Circuit Board 6 Test

All measurements are relative to OV "MYTCHETT" with oscilloscope settings of [\div], [\div], [trigger=].

- \* Check that the printed circuit board is correctly connected to the following: Printed Circuit Board 5 via PL501, PL502 Ratio/Reference socket via PL603
- \* Switch the voltmeter on and connect an oscilloscope (set to 500mV, 2ms, Line) to TP402 "CHOPPER O/P". The observed results should be in the ranges: spikes <1V peak noise <0.5V peak
- \* To check the main amplifier offset, connect a digital voltmeter (set to Vdc) to TP403 "DEMOD O/P". The digital voltmeter result should be: -10V < reading < +10V
- \* To set the ac offset voltage, connect the digital voltmeter (set to Vdc) to TP705 "BUFFER O/P" and adjust RV701 until  $-100 \mu V < \text{reading} < +100 \mu V$ .
- \* Connect the calibrator Low to Sl right second pin back and calibrator High to Sl left, second pin back. With the digital voltmeter set first to Vdc, check the ranges shown below:-

7081 Setting	Expected Digital Voltmeter Result
100mV, 1V, 10V dc 100V dc 100mV, 1V, ac 10V ac	Zero < $10\mu V$ , full scale +0% to +4% Zero < lmV, full scale +0% to +4% Zero < $500\mu V$ , full scale +0% to +4% Zero < $50m V$ , full scale +0% to +4%

- \* Connect a lV, lkHz source and press the 7081 front panel V~ control. With an oscilloscope (set to 20mV, 5ms, External) connected to TP752 ~- "CHOPPER BALANCE", trigger from R779, adjust RV751 "BALANCE" until the flattest trace is achieved.
- \* Connect a IV, 100kHz source and adjust RV752 to give a reading of 1.00000 ± 20 bits.
- \* Connect a lV, lMHz source and adjust RV753 to give a reading of 1.00000  $\pm$  100 bits.
- \* Repeat the previous two steps.

## 9.6 Assembly Check

- \* Ensure that links 1, 3, 4, 5, 6, 7 and 8, on printed circuit board 3, are installed.
- \* Check that the following split pads, on printed circuit board 5, are made: 201, 202, 501, 801, 802, 803, 804, 805, 806, 807, 808, 809, 901, 902, 903, 904.
- \* Set the mains power selector to 240V and check that a 200mA fuse is installed.
- \* Set the GP-IB address to 18, ie

	х	x	x	х	x	x	x	ON OFF
^		Λ	Λ		Λ.	Α		Oter

\* Set S1, on printed circuit board 3, as follows:-

$\left  \frac{\mathbf{x}}{\mathbf{x}} \right $	OFF
$\left  \frac{\mathbf{x}}{\mathbf{x}} \right $	
X	
X	
<u>x</u>	
<u> </u>	
<u>x</u>	
	$\frac{\overline{x}}{x}$

- \* Check that the shorting clip (printed circuit board 3) has been removed from TR2.
- \* Set Sl. on printed circuit board 5, as follows:-

	6801µP		(	6303µP	
ON	$ \begin{array}{c c} \hline x \\ \hline x \\ \hline x \\ \hline x \\ \hline x \end{array} $	OFF	ON	X   X   X   X   X   X   X   X   X   X	OFF

\* Check that printed circuit board 3 is connected to the following:-RUN/CAL switch via PL3 Keyboard via PL2 Printed Circuit Board 1 via PL6 Printed Circuit Board 5 via SK51 RS232 Socket via PL5 Minate Socket via PL4 Transformer via PL51, PL52 Beeper via TP3, TP4 OV Earth via TP53.

- \* Check that printed circuit board 4 is connected to the following:Printed Circuit Board 8 via SK414.

  GP-IB Socket via SK412
  Printed Circuit Board 3 via PL1:
- \* Ensure that printed circuit board 5 is connected to printed circuit board 3 via SK901. Also check that the orientation of IC801 and IC826, on printed circuit board 5, is correct, as their orientation should be the reverse of all the other ICs.
- \* Ensure that the shorting clips are removed from TR203, TR204, TR603, TR605, TR610 (printed circuit board 5).
- \* Check that printed circuit board 6 is connected to the following:-Printed Circuit Board 5 via PL501, PL502, PL504. Ratio Socket (High, Low) via PL603 (TL1, TL2).
- 9.7 Power Supply and Digital Checks
- \* Connect the 7081 power input to a variac and gradually increase the input to 240V. "NVM FAIL" should be displayed but "CAL INCOMPLETE", "INITIALISED or "RESUMED" are also acceptable.
- \* Check that there are no missing or additional display segments.
- \* Check the keyboard operation by pressing each key and listening for a "beep".
- \* Ensure that the LED annunciators work.
- \* Press "initialise" followed by "DIG FILT". The "compute" LED should light.
- \* Press "V——" followed by "V". The second beep should be twice as long as the first.
- \* Connect the 7081 to a variac source. Set the variac first to 216 and then to 264V, and check, using a digital voltmeter, that each of the following test point voltages is within the stated range:-

Printed Circuit Board	Measure Across	Low Mains Input	High Mains Limit
3	TP53-56 TP54-55 TP53-IC52 pin l TP53-D58 cathode TP53-D53 cathode TP53-D60 cathode TP53-D61 anode	24 24 38 4.75 4.75 11.4 11.4	35 35 42 5.25 5.25 12.6 12.6

Printed Circuit Board	Measure Across	Low Mains Input	High Mains Limit
5	TP903-D904 cathode	29	45
	TP903-901	25.6	28.4
	TP903-902	14.2	15.8
	TP903-904	-14.2	-15.8
	TP903-906	-25.6	-28.4
	C609	36	53
	TP604-606	35	39
	TP604-603	-23.7	-26.3

- \* Connect normal 240V ac mains power (increase mains from zero using a variac each time) and check that the voltage across IC901 left hand pin and TP903 is not less than +17.5V. Repeat test with 198V ac input on the 220V setting.
- \* Change to a 400mA fuse and repeat step 8 for 108V ac input on the 120V ac setting and 90V ac input on the 100V ac setting.
- \* Refit 200mA fuse and return to the 240V setting.
- \* Connect a Silent 700 to the RS232 port. Set the Silent 700 NUM, LOW SPEED and HALF DUP switches OFF and the ON LINE switch ON.

Type: OUT, RS, ON: MEAS, SING

One result should be printed out.

\* Connect frequency counter ground to printed circuit board 3 TP2 and probe TP1. Adjust C3 for a frequency in the range of 32767.99 to 32768.01Hz.

Set up date by typing on the Silent 700, for example: DATE = 14,3,83

Set up the time by typing, for example: TIME = 14,22

Check that the values have been accepted by typing

TIME?:DATE?

\* Press "initialise". The display should return with "NVM FAIL".

## 9.8 Analogue Checks

- \* Phase Locked Loop Frequency Set a bench supply to +2.5V. Connect the low terminal to TP904 and the high (+2.5V) to the negative end of C806. Connect the low terminal of a frequency counter to TP904 and probe IC835 pin 5. Adjust C807 for a frequency between 5.21MHz and 5.27MHz.
- \* Using a high impedance voltmeter (e.g. 7060) monitor the voltage at the negative end of C806 with respect to TP904. The voltage should settle to  $2.5V \pm 0.3$ . Adjust C807 to correct, if necessary.

Disconnect the bench supply and switch on the 7081 using 60Hz mains frequency. Check that, after settling, the voltage on C807 is 2.5V  $\pm$  0.5.

\* Reference Voltage Connect the 7060 between TP302(+10V) and TP303(-10V), ensuring that LK301 and LK302 are configured as follows:-

Voltage	LK301	LK302
19.7-20V	OPEN	OPEN
20-20.31V	OPEN	BRIDGED
20.31-20.63V	BRIDGED	OPEN
20.63-20.96V	BRIDGED	BRIDGED

\* D-A Converter Check the operation of the digital-to-analogue converter by connecting a 7060 to TP305(0V) and TP301 "CURRENT". Switch 7081 to CAL (front panel key): Type:

CALIBRATE, ZENER, 064

and wait for the command to be executed.

Press "initialise" on the front panel.

The 7060 should read <10mV

Now type:

OUT,RS,ON CALIBRATE,ZENER,124

and wait for the commands to be executed.

Press "initialise". The 7060 should read  $-9.18V \pm 0.2V$ .

\* Connect scope ground to the printed circuit boards OV level, (scope should be set to 5V, 2ms, AUTO) and probe TP204 "GLUGS".

Short circuit the 7081 input. The waveform should have a period of 6.25 ms.

Type : MODE, TEST 0:NINES, 3

The period should reduce to 1.56ms.

Set scope to 5V, 100ns, AUTO and check that each edge has a rise or fall time of <300ns and that the gap time is 13  $\pm$   $3\mu s.$ 

\* Check that the voltage across R355 is less than 100µV at room temperature.

## CHAPTER 10

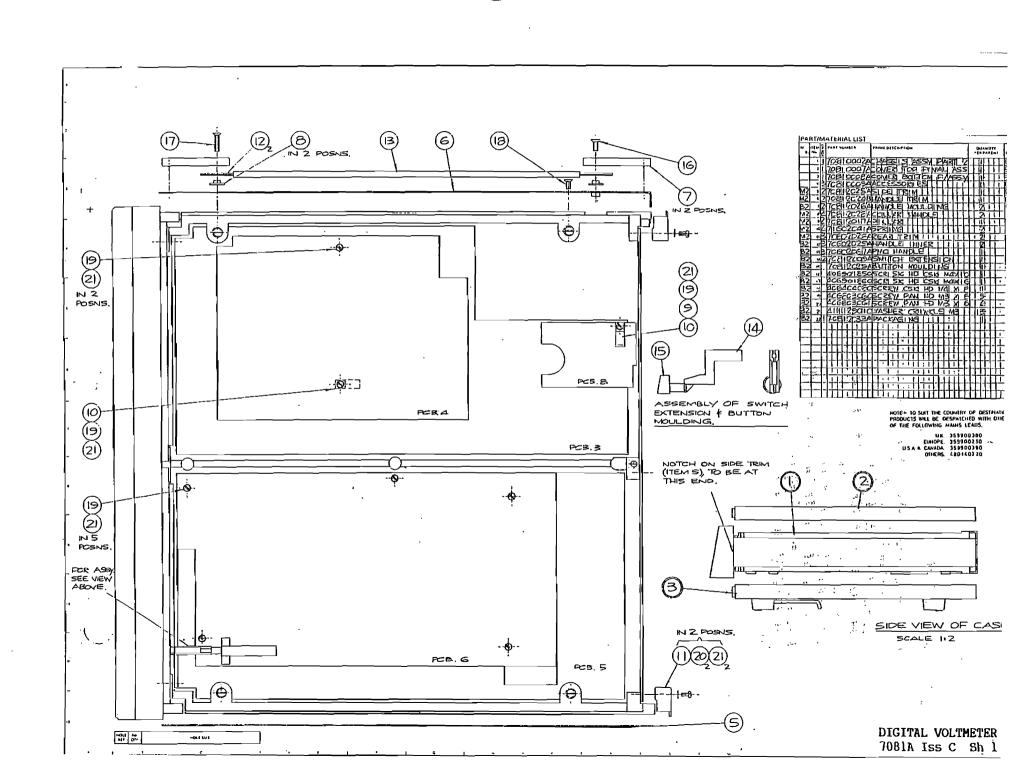
# Instrument Assembly Parts CONTENTS

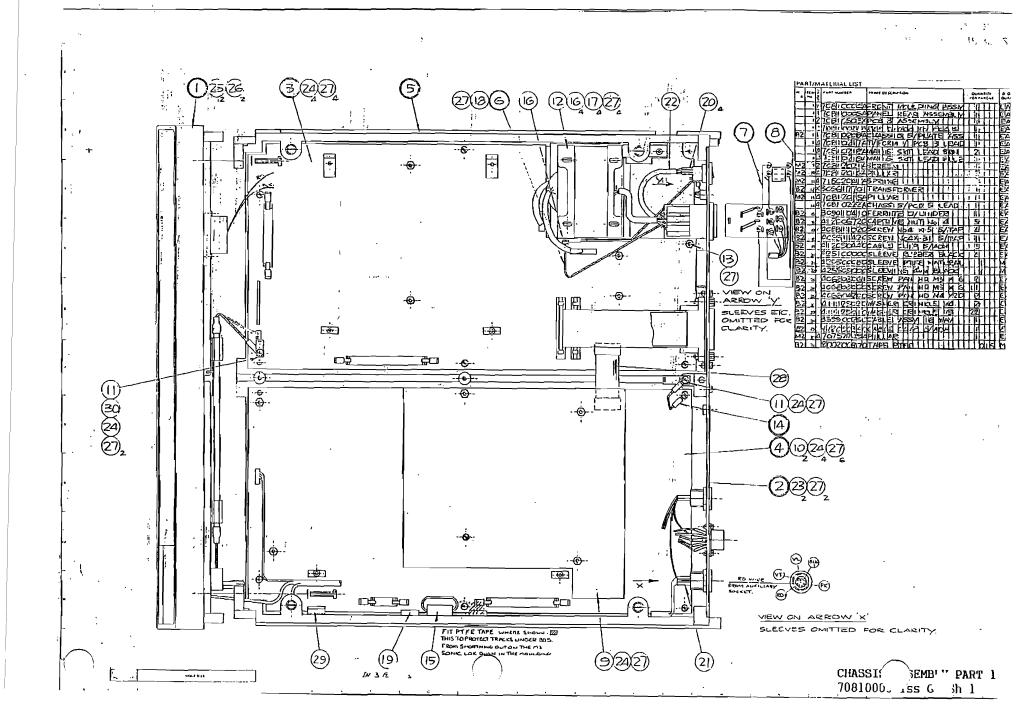
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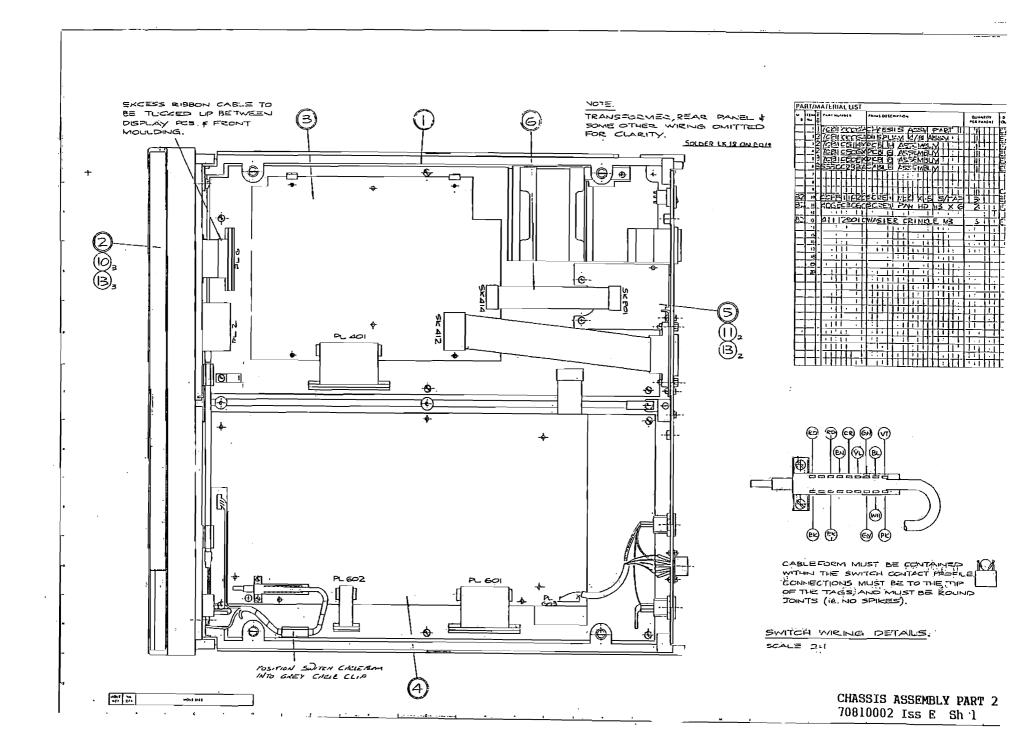
## 10.1 INTRODUCTION

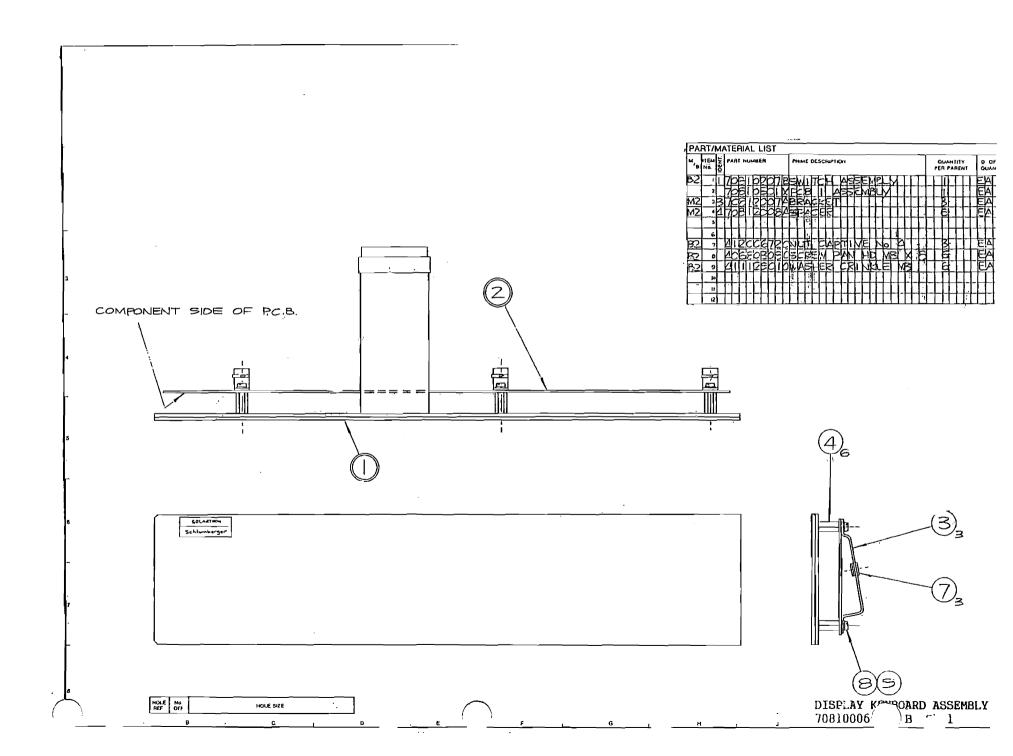
This chapter contains detailed engineering drawings for all of the main assembly parts of the 7081/7071 digital voltmeter. The components that make up each assembly part are referenced with an item number which corresponds to a Solartron part number, given in the Assembly Parts List.

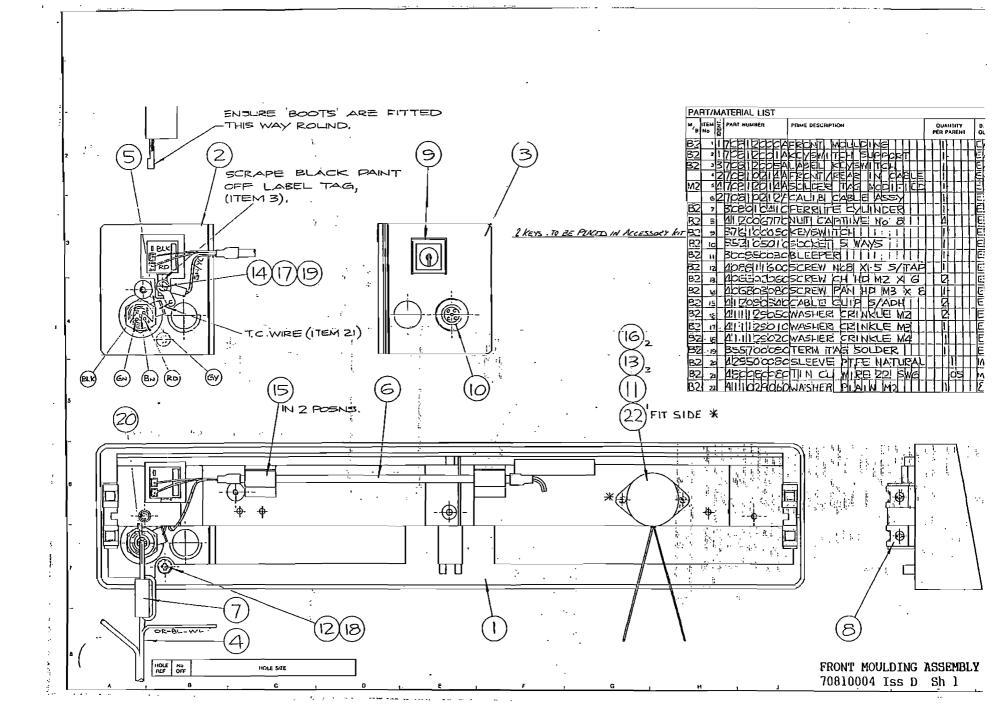
When ordering spare parts it is essential to quote the instrument serial number, located on the rear panel of the instrument, as well a full description of the assembly drawing and the component part required in that drawing.

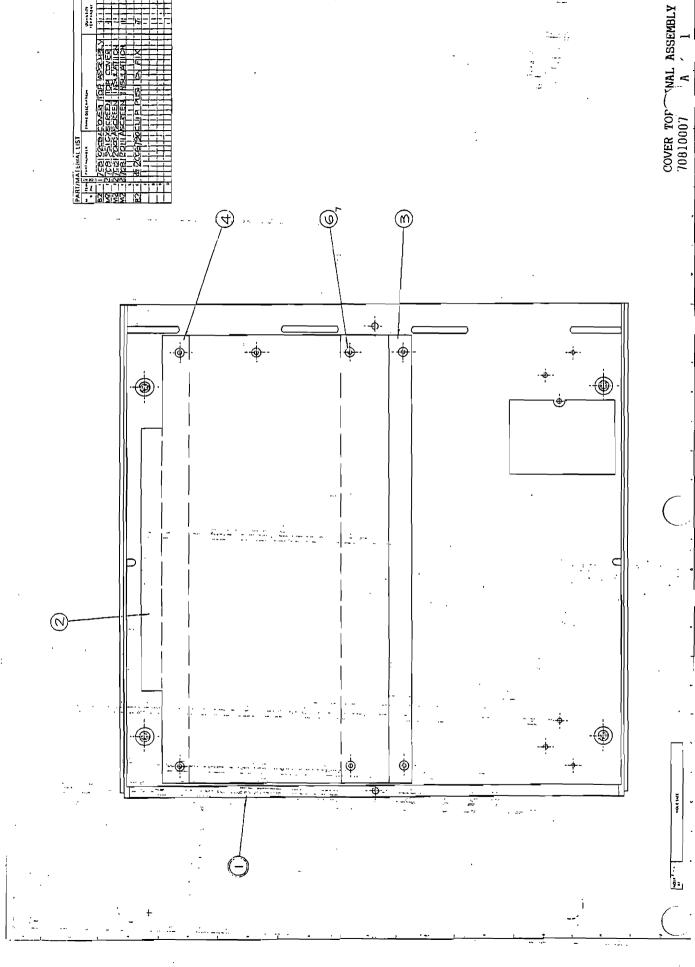


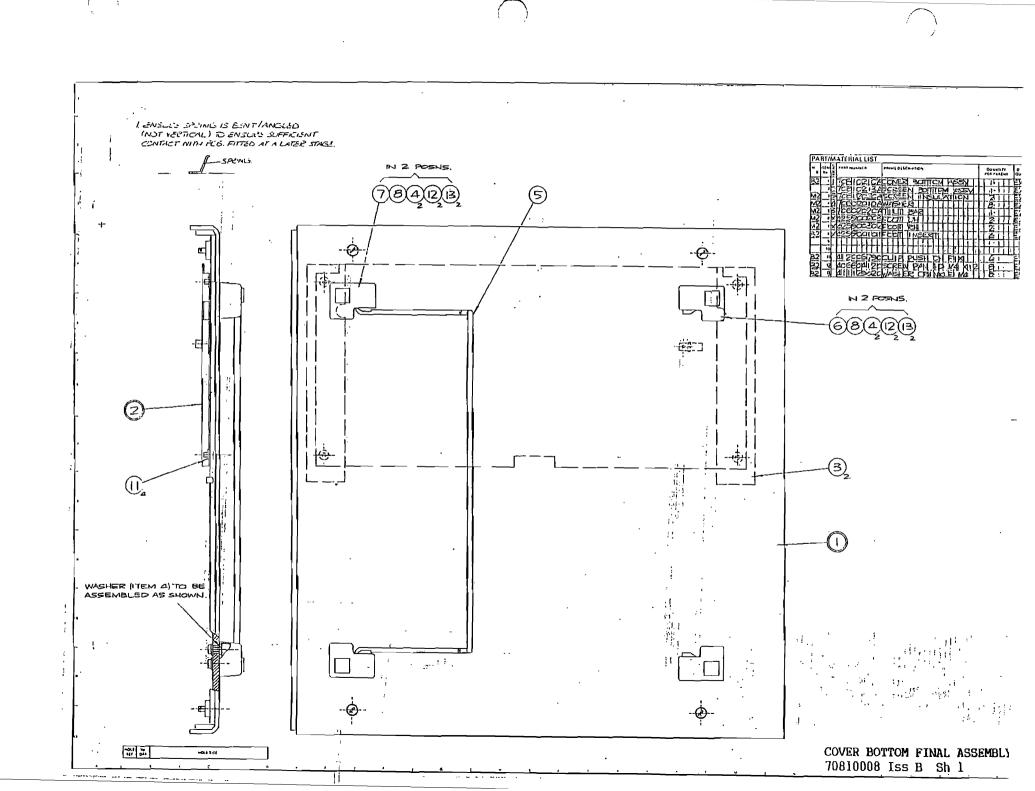


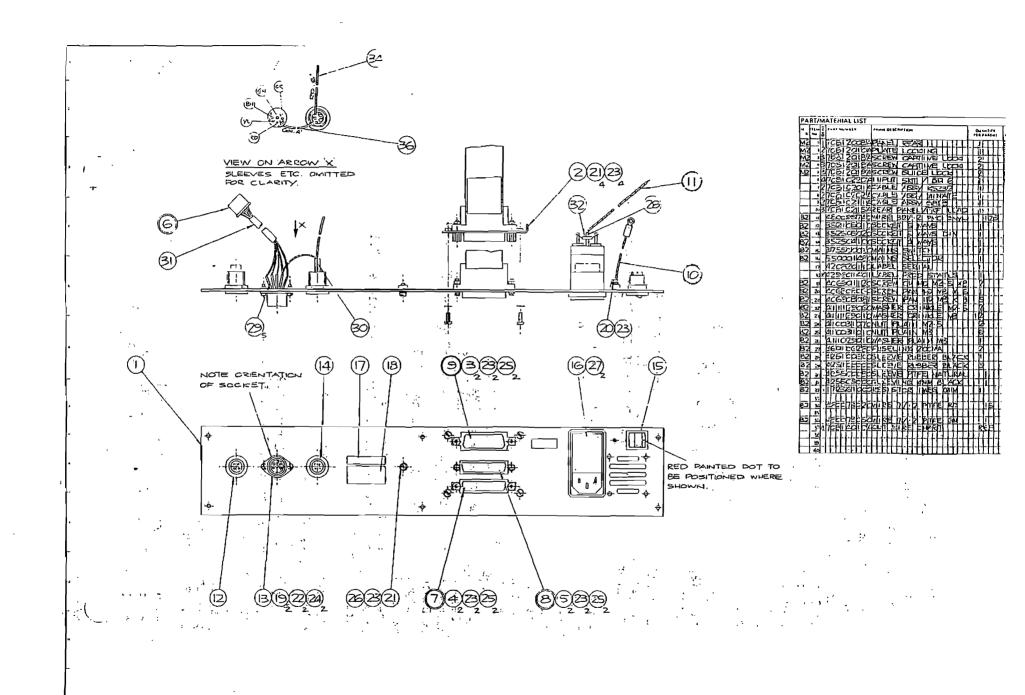












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